2-P(MIX)

CR-122416

FROM···Magnavox RESEARCH LABORATORIES

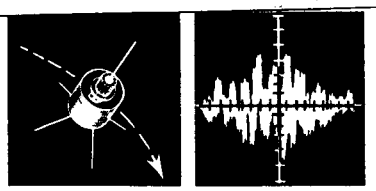
TORRANCE • CALIFORNIA

OPERATION MANUAL

FOR

MX-290 DATA-VOICE PN MOD

MX-291 DATA-VOICE PN DEMOD



THE MAGNAVOX COMPANY···GOVERNMENT AND INDUSTRIAL DIVISION

OPERATION MANUAL

FOR

MX-290 DATA-VOICE PN MOD

MX-291 DATA-VOICE PN DEMOD

Contract No. NAS5-16955

Prepared for

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Prepared by

Magnavox Research Laboratories
2829 Maricopa Street
Torrance, California 90503
(213) 328-0770

MRL Report No. R-4165
11 October 1971

ABSTRACT

This operation manual is also the final report of the work performed under Contract No. NAS5-16955. The objective of the program was to design, assemble, checkout, and deliver to the customer three MX-290 transmitters and two MX-291 companion receivers. These units are based on modifying the MX-170B subunits wherever feasible so as to perform in accordance to NASA Specification No. 70327-1 dated 23 February 1970. These equipments were designed and assembled to provide for maximum flexibility with respect to making changes in electrical circuits which may be required for future applications. A number of test points for monitoring and troubleshooting were provided along with easy access to subunits.

Section I of this document is the introduction. An introduction to spread spectrum communication techniques is presented in Section II for readers unfamiliar with the subject. Section III presents a system description of the MX-290 transmitter and MX-291 receiver. The detail implementation of the units is found in Section IV. The schematic diagrams are placed in Section V; Section VI covers any necessary alignment procedures; recommendations are presented in Section VII.

Appendix A lists symbols that were used throughout this document along with their definitions. Final acceptance test data is included in Appendix B.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

SECTION I

INTRODUCTION

1.1 GENERAL

This operation manual is deliverable item No. 3 of Contract NAS5-16955 and is also the final report of the program.

Under Contract NAS5-16955 to NASA, Magnavox Research Laboratories (MRL) designed and fabricated three MX-290 Data-Voice PN Modulators and two MX-291 Data-Voice PN Demodulators. Originally, the equipment items were to be modified versions of Magnavox Model MX-170B Transceiver. However, because of the extensive circuit modifications that were required to meet NASA specification No. 70327, it turned out that only a limited number of the original MX-170B plug in modules could be reworked for use in the deliverable equipment. Furthermore, because the final units have very little resemblence to the MX-170B, they were given their own nomenclature, MX-290 and MX-291.

The MX-290/291 Data-Voice Process Mod/Demod are spread spectrum modulation/demodulation units designed to provide a push-to-talk, half duplex, communications link or data link at 2400 or 1200 bps with a 70 MHz IF interface for both the MX-290 transmitter and the MX-291 receiver. The MX-290/291 Data-Voice Mod/Demod shown in figure 1-1 exhibits the following operational characteristics:

- Speech privacy
- Digital data transmission and reception at 1200 and 2400 bps
- Discrete address and multiple access

1.2 SPEECH PRIVACY

Concealment of the signal message content is achieved by the method of pseudonoise (PN) modulation, which prevents recovery of any intelligence until the received signal has been correlated with a matched reference. The audio signal is converted to a pulse duration modulated (PDM) digital bit stream that is added

971-1679
UNCLASSIFIED

Figure 1-1. MX-290 and MX-291 Equipment

modulo-two to the pseudorandom code; thus, the system provides privacy of communication, which is extremely useful for short-term protection of information against unauthorized reception.

1.3 DIGITAL DATA OPERATION

This system provides a capability for transmission and reception of digital data at bit rates of 1200 and 2400 bps. Synchronous data clock signals are provided by both the MX-290 transmitter and MX-291 receiver equipment. A spread spectrum system employing a correlation-detection process with a replica of the transmitted PN signal requires that the receiver be in time synchronism with the required signal before demodulation can occur. Since this synchronization is required for communication, it is applied advantageously for other purposes such as the generation of synchronous transmit and receive data clock signals.

1.4 DISCRETE ADDRESS AND MULTIPLE ACCESS

Because the receiver must be in possession of the matching reference code pattern, the spread spectrum system can provide the discrete address capability, whereby a transmitter can select a particular receiver by choice of PN sequences.

In addition, the system enables access on a common channel since the use of distinct sequences means that one PN signal acts as interfering noise to another PN signal. This being the case, a number of signals can occupy the same frequency channel at one time with minimum mutual interference up to the multiple access margin of the system.

These units provide 8192 quasiorthogonal PN sequences via front panel access. All of these sequences have good auto-and cross-correlation properties.

SECTION II

INTRODUCTION TO SPREAD SPECTRUM TECHNIQUES

This section describes the basic theory of spread-spectrum communication systems using pseudorandom noise modulation. Readers not familiar with the subject techniques will find this section helpful in understanding the subsequent sections of this manual.

2.1 ADVANTAGES OF SPREAD SPECTRUM MODULATION TECHNIQUES

The application of spread spectrum modulation techniques to communication systems provides certain capabilities which cannot be realized through conventional modulation techniques. The primary advantage provided by spread spectrum modulation is the capability of a communication system to reject interfering signals or "jamming" and to recover the desired signal. This "anti-jam" capability is of great significance to communications because it provides a large measure of protection from active enemy countermeasures, message privacy, increased transmission reliability, and immunity to selective fading.

Spread spectrum (pseudonoise) modulation results in a wide-band, low-power-density signal which has statistical properties similar to random noise. As a result, the transmitted signal is not readily detected or recognized by conventional passive countermeasures (surveillance). Recovery of the baseband information from the wide-band transmitted signal can be accomplished only through correlation with a stored reference which is an exact replica of the transmitted signal. This property denies the casual listener access to the baseband information. Therefore, spread spectrum modulation provides message privacy.

Because of the correlation detection techniques employed in the wide-band mode, accurate range measurements between two communicating stations can be made by measuring the time displacement between a transmitted code and the corresponding code generated by the receiving station. This measurement is then translated to miles and displayed on a range indicator.

When the preceding advantages are considered, the desirability of spread spectrum modulation in satellite communication systems is quite apparent.

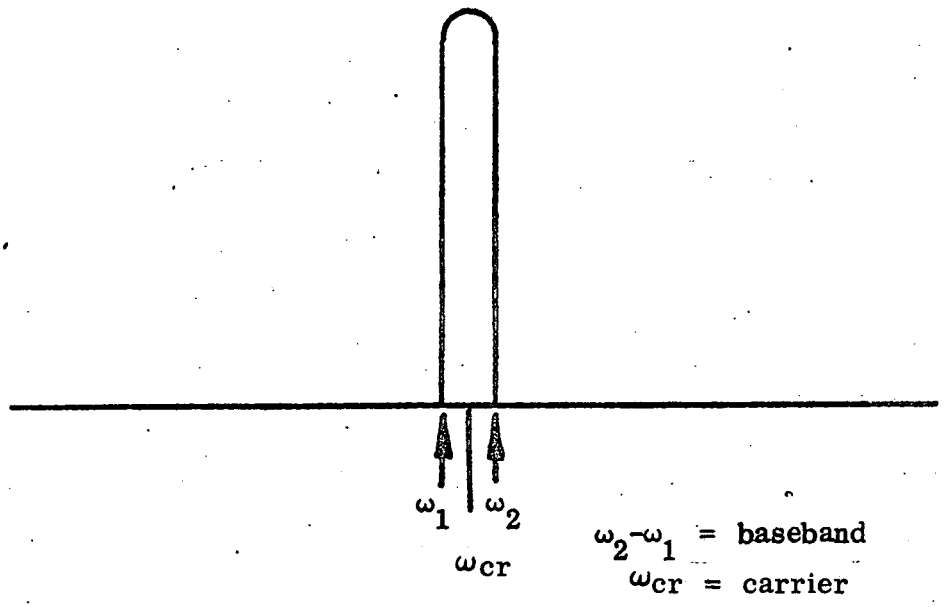
2.2 POWER SPECTRUM

Figure 2-1 compares the power spectrum of a conventional narrow-band transmission and a spread spectrum transmission. In conventional frequency modulation, the transmitted signal occupies a bandwidth roughly equal to twice the highest modulating frequency plus the peak-to-peak frequency deviation. All the transmitted power, therefore, is contained in a comparatively narrow band of frequencies. In spread spectrum transmission, the transmitted signal occupies a bandwidth many orders of magnitude greater than the baseband information. Therefore, for the same transmitted power the same base bandwidth, the spectral power density of the spread spectrum transmission will be many orders of magnitude less than the conventional signal. Further, the spread spectrum signal will have statistical properties closely approximating those of random thermal noise.

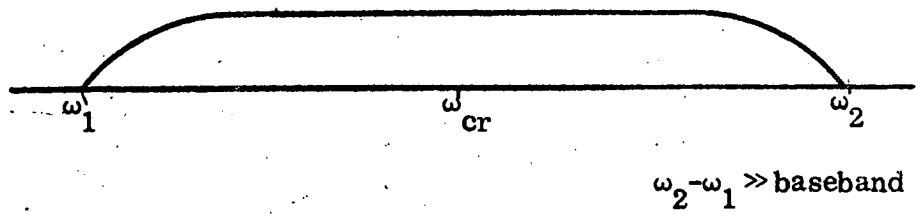
2.3 PSEUDONOISE GENERATOR

Implementation of a spread spectrum communication system requires the generation of a signal of extremely wide bandwidth which has the statistical properties of random noise. Since this signal must be systematically generated, it has been termed pseudorandom or pseudonoise. The optimum method for generating a pseudonoise signal is through use of a pseudorandom binary sequence generator, a simple version of which is shown in figure 2-2. This generator consists of a series of storage elements, or flip-flops, and in this respect it is identical to the shift register employed in digital computers. Each flip-flop is connected in such a manner that the content of each stage is transferred to the succeeding stage upon the occurrence of a clock pulse.

The pseudorandom binary sequence generator differs from the shift register used in computers in that the output of two or more stages is processed and fed back to the input of the first stage. The feedback operation is that of modulo-two addition. This is performed by an exclusive-OR gate. The operation of this feedback network is such that a logical "one" is produced if the inputs to the exclusive-OR gate are different, i.e., a "one" and a "zero" or the reverse. The output of the exclusive-OR gate is a logical "zero" if both inputs are the same. With proper location of the feedback lines from the register stages to the exclusive-OR gate, the shift register generator will produce a binary sequence which has a length of 2^n-1 bits before it

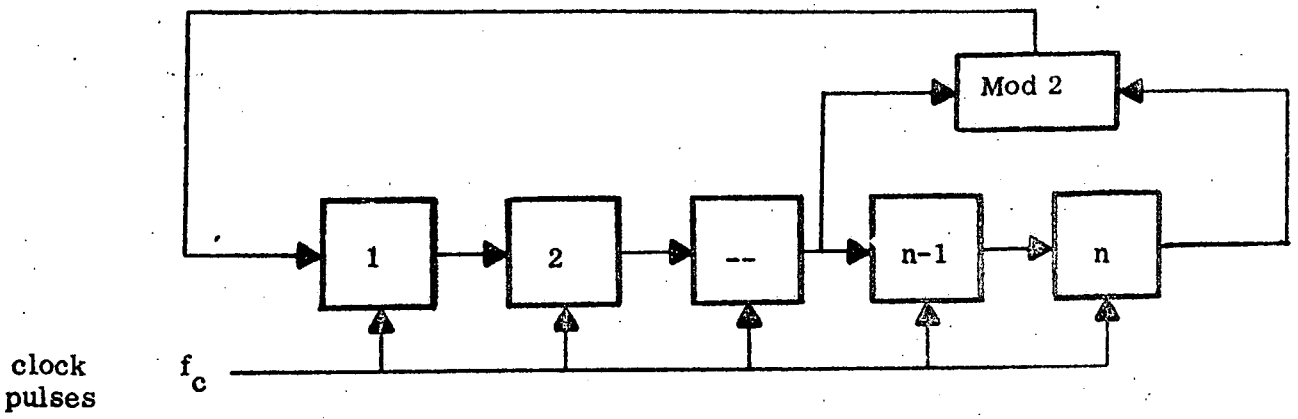


(a) Conventional Narrowband Signal



(b) Spread-Spectrum Signal

Figure 2-1. Comparison of Power Spectrums of Narrowband and Spread-Spectrum Signals



$$N = 2^n - 1$$

N = MAXIMUM NUMBER OF BITS BEFORE SEQUENCE REPEATS

n = NUMBER OF STAGES IN THE SHIFT REGISTER

EXAMPLE: n = 20 $2^n = 1048576$

$N = 1048575$

IF f_c = 1 MC

SEQUENCE REPEATS IN ≈ 1.05 SECONDS

Figure 2-2. Pseudonoise Generator

repeats. (n represents the number of shift register stages.) For n = 5, the sequence produced will be $2^5 - 1$, or 31 bits. From this it can be seen that extremely long sequences can be produced by merely adding more stages. For example, if 20 stages are used, the sequence will contain approximately 10 bits. The precise order in which the "ones" and "zeros" occur is dependent upon the feedback connections. The distribution of "ones" and "zeros" in a sequence is "normal" and, therefore, these sequences are known as pseudorandom binary sequences. Various sequences can be obtained from the same register by connecting the feedback taps to different stages and using more than two feedback taps.

The type of binary sequence produced by the shift register generator shown in figure 2-2 is pictorially illustrated in figure 2-3. Also shown in figure 2-3 is the power spectrum of the pseudorandom binary sequence. When modulated on a carrier, the nominal RF bandwidth equals the code rate, since the power outside this bandwidth is relatively small.

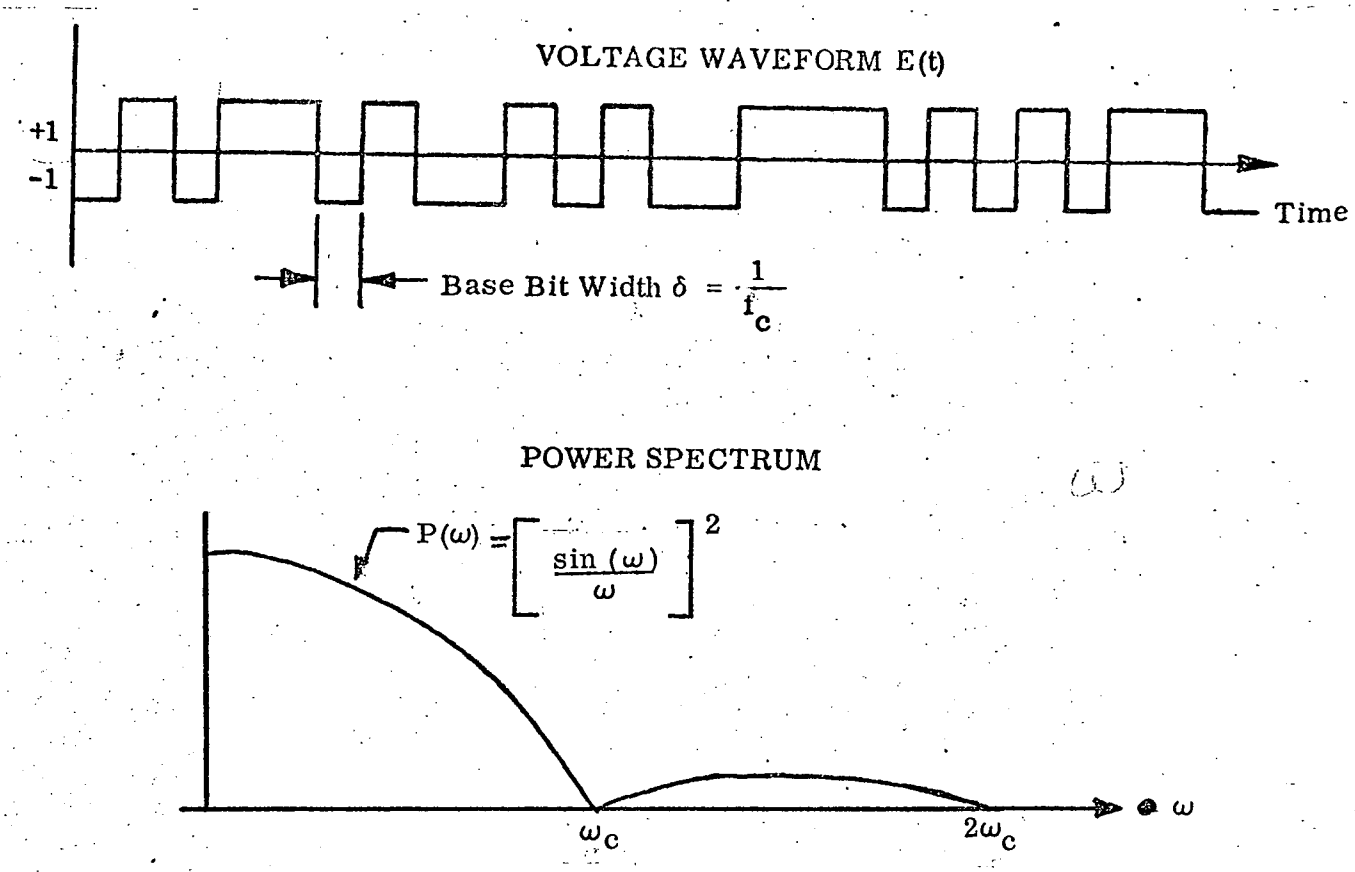
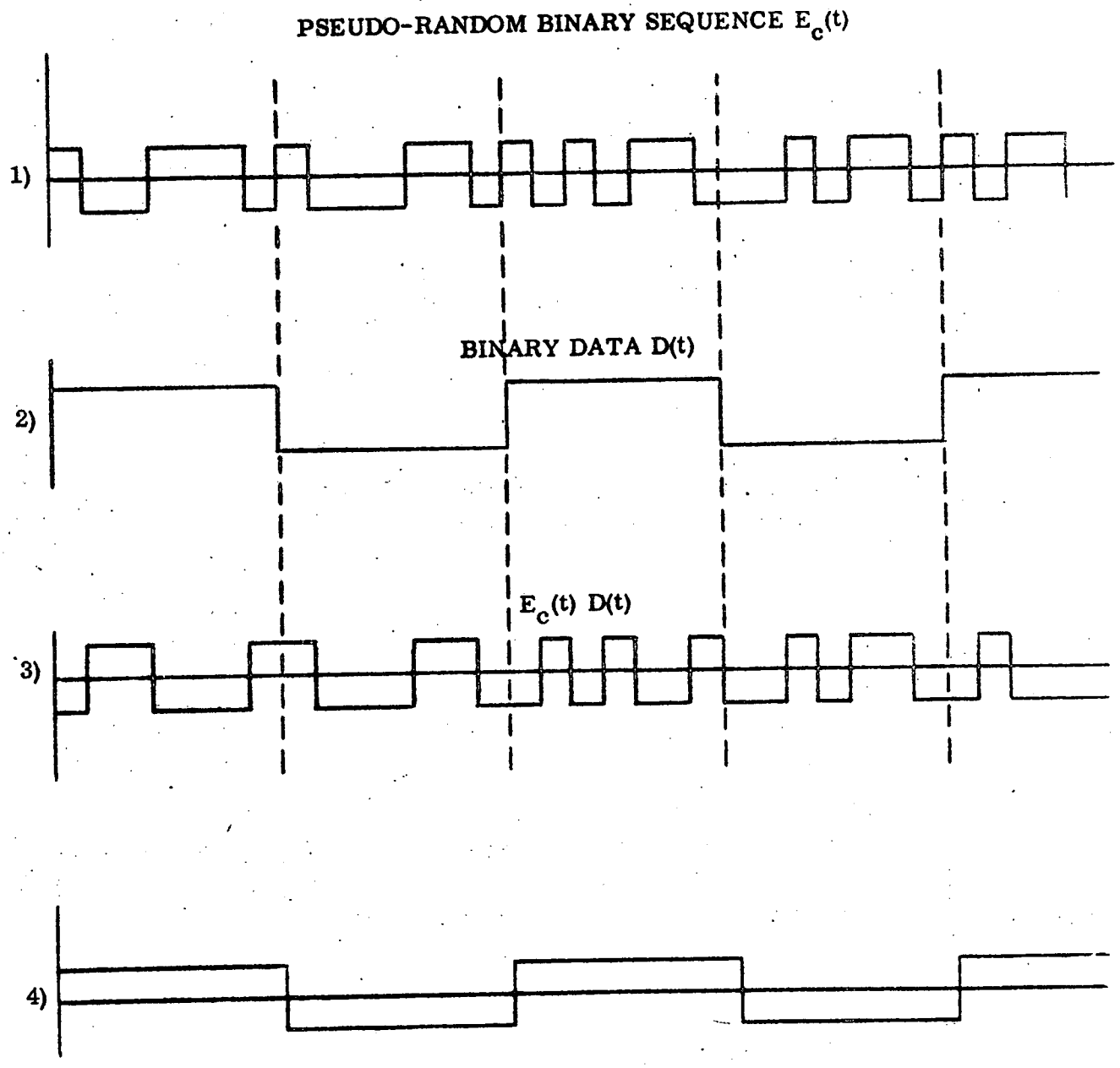


Figure 2-3. Output Voltage Waveform of a Pseudo-Noise Generator and the Power Spectrum of a Wideband Signal

2.4 DATA MODULATION OF PSEUDORANDOM SEQUENCE

Having generated the wide band noise like signal, the next process to consider is the addition of intelligence or baseband to the spread spectrum signal. As shown in the previous figure 2-3, the signal is a pseudorandom binary sequence. Addition of the baseband information to the pseudorandom sequence is accomplished through the process of binary or modulo-two addition. This is depicted in figure 2-4. Waveform #1 is the pseudorandom sequence which is represented mathematically by the expression $E_c(t)$. The baseband signal or intelligence is shown as waveform #2 and is represented by the expression D(t). It is shown as a digital signal since it must be in digital form for addition to the pseudorandom sequence. Accordingly, if analog data is to be transmitted, it must first be converted to digital form. The resulting signal is shown as the third waveform on the chart. Examination of this waveform will reveal that this process causes the pseudorandom sequence to be inverted (complemented) at the data rate. That is, when the data signal is a logical "one", the "ones" and "zeros" in the sequence are inverted. When the data signal is a logical "zero", the "ones" and "zeros" in the sequence are unaltered.



$$E_c(t)\ D(t)\ E_c(t) = {}^{*}E_c(t)^2\ D(t) = D(t)$$

$$* E_c(t) = +1 \text{ or } -1$$

$$\therefore E_c(t)^2 = 1$$

Figure 2-4. Data Modulation of Pseudorandom Sequence

When a sequence to which data has been added is correlated with an identical sequence which has not been perturbed by data, the polarity of the correlation output will reverse at the data rate. Hence, the data can be recovered by correlation. This is shown in waveform #4.

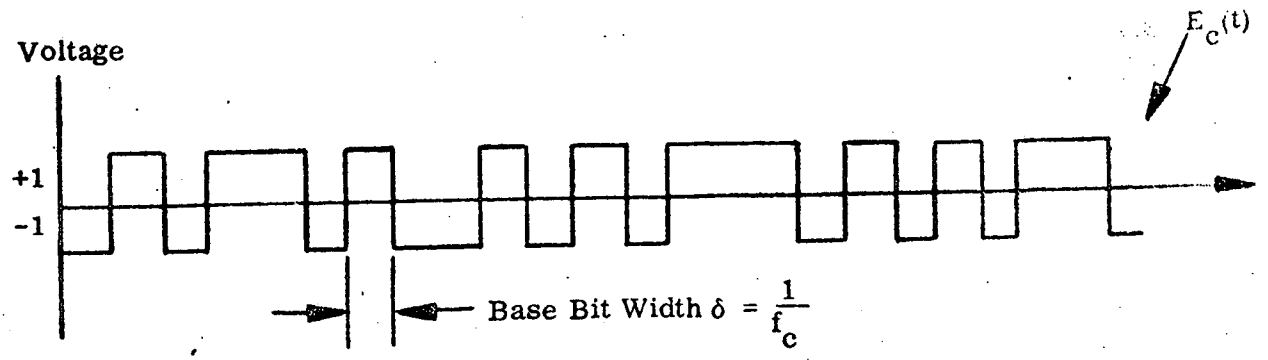
2.5 AUTO CORRELATION OF A MAXIMAL LINEAR SEQUENCE

Recovery of information on baseband data from a spread spectrum transmission is accomplished by a process known as correlation. The transmittal spread spectrum signal is multiplied with a stored reference signal at the receiver. The signal resulting from the correlation process is appropriately filter (integrated). Hence, the term correlation which means the average product or the integral of the instantaneous product of the two signals.

When a signal is correlated with itself (or an exact replica) the process is known as auto-correlation. Ideally a spread spectrum signal should exhibit a maximum correlation with itself and a minimum correlation with all other classes of signals. A pseudorandom binary sequence of the maximal linear type has such correlation properties as shown in figure 2-5. This property is essential to the jamming rejection capability of a spread spectrum system.

When a spread spectrum (pseudonoise) signal is correlated (multiplied) with another signal, the result will be a pseudonoise signal except for the unique case when the signal with which the pseudonoise signal is multiplied is an exact replica of the pseudonoise signal and is exactly in phase. Under these conditions we have auto-correlation. The pseudonoise signal is essentially squared and the result is a DC term with a relative amplitude of one (1). For all other phases of the replica signal and all other classes of signals, the correlation process yields a pseudonoise signal of relative amplitude equal to the reciprocal of the pseudorandom binary sequence length (i.e. $\frac{1}{2^n - 1}$. This is shown graphically on the lower half of figure 2-5.

In the case where the transmitted signal has been modulated with data, figure 2-4, the correlation process yields a DC term whose polarity will reverse at the data rate.



$$\phi(\tau) = \frac{1}{t} \int_0^t E_c(t)\, E_c(t+\tau)\, dt \qquad \tau$$

τ = Delay in bit increments

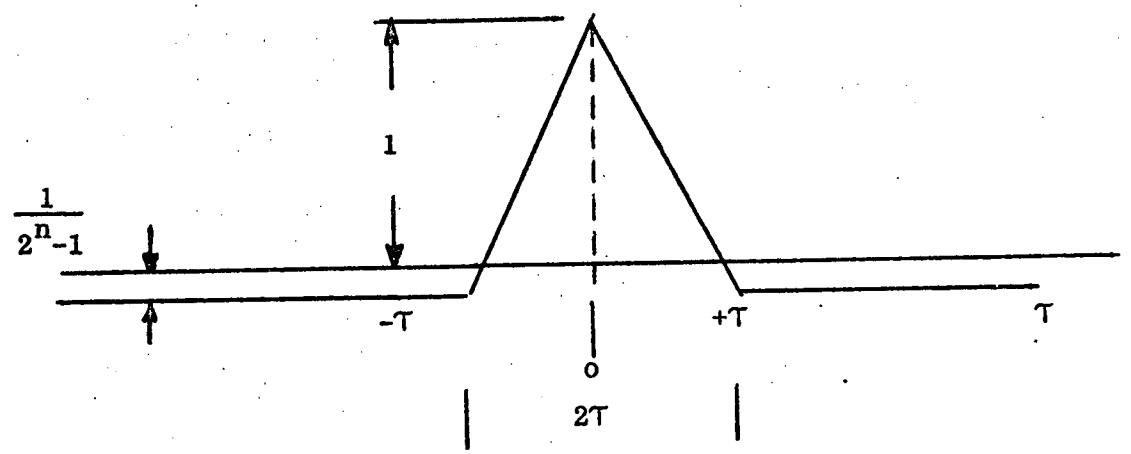


Figure 2-5. Auto-Correlation Properties of a Linear Maximal Sequence

2.6 BASIC DIRECT SEQUENCE SPREAD SPECTRUM SYSTEM

Figure 2-6 illustrates the essentials of a basic direct sequence type spread spectrum (pseudo-noise) communication system. Looking first at the transmitter we see that the basic elements are the pseudo-random binary sequence generator, data modulator, binary encoder and balanced modulator. The sequence generates a maximal linear pseudo-random binary sequence. The baseband information if binary is applied directly to the data modulator. If analog, the baseband information is first converted to binary form and then applied to the data modulator. The binary or binary encoded data is added to the binary sequence by modulo-two (binary) addition. The process yields a signal represented by $E_c(t)\ D(t)$. This signal is then fed to the balanced modulator where it balance modulates a local oscillator signal $\cos \omega_1 t$. This yields a double sideband suppressed carrier spread spectrum signal represented by $E_c(t)\ D(t) \cos \omega_1 t$.

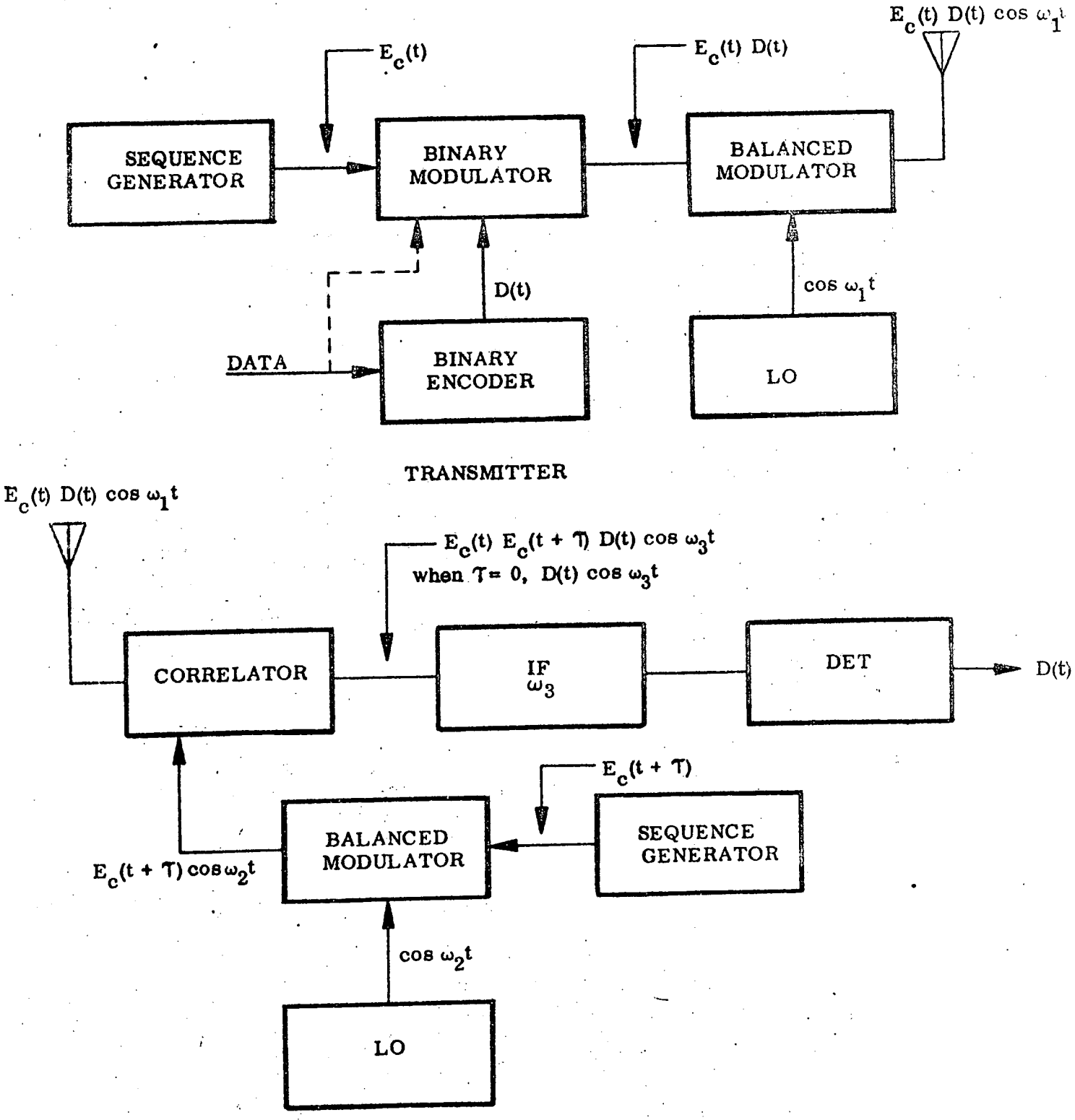


Figure 2-6. Basic Direct-Sequence Type Spread Spectrum System

Examine next the receiver. Here we see the basic elements which are the correlator, sequence generator, balanced modulator, IF strip and detector. The sequence generator produces an identical pseudo-random binary sequence as was produced by the transmitter. This is represented by $E_c(t+\tau)$. The τ term indicates an initial arbitrary phase relationship since the transmit and receive sequences are generated independently. The signal $E_c(t+\tau)$ balance modulates the receiver local oscillator producing a double sideband suppressed carrier (biphase) spread spectrum (pseudo-noise) signal represented by $E_c(t+\tau) \cos \omega_2 t$. This signal is then correlated (multiplied) with the incoming signal and the difference frequency term is selected by filtering. This signal is $E_c(t+\tau)\ D(t)\ E_c(t) \cos \omega_3 t$. The phase of the locally generated sequence (stored reference) is varied until $\tau = 0$. At this point the correlator output is $E_c^2(t)\ D(t) \cos \omega_3 t$. Since $E_c(t) = +1$ or -1, then $E_c(t)^2 = 1$; therefore, when $\tau = 0$, the output of the correlator is $D(t) \cos \omega_3 t$. This is a PSK signal and is reversing phase at the data rate. This signal is subsequently detected yielding the data D(t).

SECTION III

SYSTEM DESCRIPTION

3.1 GENERAL

The MX-290 modulator and the MX-291 demodulator form a modem with a 70 MHz carrier interface. The MX-290 performs the transmitter operation and the MX-291 functions as the receiver. Input data is digital at 1200 or 2400 bps, or analgo optimized for speech in the 300 to 2500 Hz range. This system uses PN coding (8192 codes) at a 1.2 MHz bit rate to approach a 27 dB or 30 dB processing gain. The 8192 codes are obtained via the front panel code select switches. Also, all PN code lengths are 8191 bits, which results in a run rate of 150 Hz for a 1.2 MHz bit rate clock. The 150 Hz run rate is decoded and multiplied up, to obtain the digital data clocks and PDM voice clock.

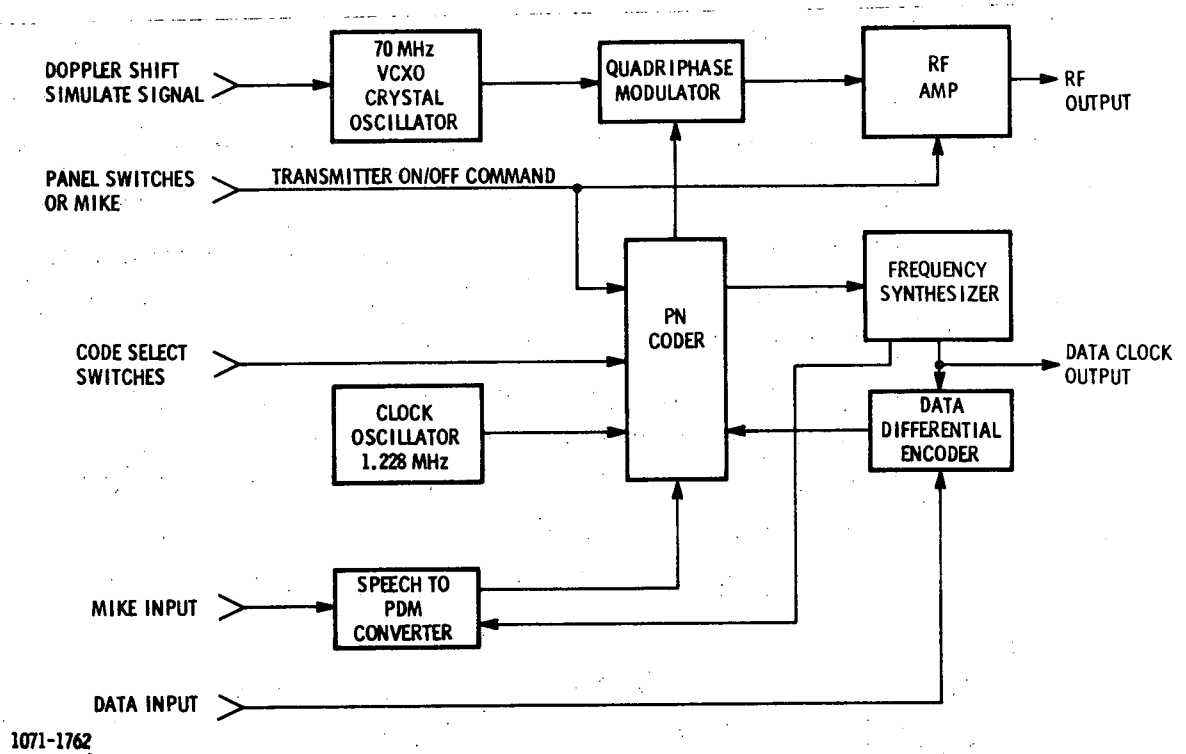
In the MX-290, transmitter, the PN encoded data signal is translated to the 70 MHz interface frequency via staggered quadriphase modulation (SQPM). The digital data is differential encoded, and the speech is suppressed clock pulse duration modulation (SCPDM) encoded, before they are mod-two added to the code stream.

The demodulation process coherent demodulates the data or voice signal after the code correlation process has been performed. Code correlation is obtained by a serial sequential decoding process. The system code tracks (maintains correlation) by detection of a prescribed intentional plus and minus incremental phase shift of the receiver coder clock (the τ jitter method). Coherent demodulation is achieved by a Costas loop. The differentially encoded digital data is extracted from the inphase channel of the Costas loop via an integrate and dump filter followed by a hard decision. The hard decision binary signal is then differentially decoded into the received digital data. The audio signal is also extracted from the inphase channel of the Costas loop. The hard decision version of the inphase channel of the Costas loop is first mod-two added with a 4800 Hz (half-clock rate) signal. This operation transforms the SCPDM to PDM. This PDM signal is converted to a PAM signal, which is then lowpass filtered and deemphasized to give the audio output signal.

3.2 MX-290 SYSTEM DESCRIPTION

Figure 3-1 is a simplified block diagram of the MX-290 unit. This simplified block shows that there are five controls or inputs and two outputs with eight functional or processing blocks. The 70 MHz output signal is a staggered quadriphase modulated (SQPM) signal formed by modulating the 70 MHz oscillator with the signal from the PN coder block. The PN coder's code is selected by the code select switches, and clocked by the 1.228 MHz oscillator. Also, the signals from the PDM converter and the data differential encoder block are transferred to the PN coder block where they are mod-two added to the code stream. The (T) transmit signal into the coder block is used to initiate the coder.

The all ones vector (Ci) is extracted from the code and goes to the frequency synthesizer where it is multiplied to obtain the clocks for the digital and speech encoders. The digital clock signal is also sent out, as an output signal. The data differential encoder converts the digital data and transfers it to the PN coder. The SCPDM encoder converts the speech to suppressed clock pulse duration modulation signal at a 9600 clock rate, and transfers it to the PN coder. The coder's code is mod-two added with the selected data and then transformed to two code streams, which are quadrature clocked versions of the same code displaced by one-half a run length. These two coders are each mod-two added to quadrature phase 70 MHz carrier signals, then summed to form the SQPM output signal.



1071-1762
UNCLASSIFIED

Figure 3-1. Block Diagram of Transmitter Unit - MX-290

The MX-290 accepts analog or digital information as inputs and transmits its PN modulated output centered at 70 MHz, and also supplies a data clock out. The basic analog input is via the noise cancelling mike connected to the mike jack input. The digital data input is via the BNC connector on the front panel or the barrier strip on the back panel. The 70 MHz carrier output is quadriphase modulated with two orthogonal, quadrature clocked Gold codes, which were mod-two added with the encoded data. The encoded data is either differentially encoded digital data or suppressed clock pulse duration (SCPDM) encoded speech. The digital data input is at 1200 or 2400 bps via MIL-STD-188B. This unit supplies a clock output via MIL-STD-188B of 1200 or 2400 bps for synchronizing external systems so that only a static phase error will occur between incoming data and data clock.

This unit transmits only when either the remote transmit line signal (TXR) located on the rear panel barrier strip is grounded, or (TXL), the transmit button on the mike is pressed or the front panel Tx/STD-BY switch is set to Tx. Also, for the first eight seconds of transmit, the data will be inhibited, allowing the system to transmit code modulated carrier only.

The Gold code is composed of two preferred pairs, 13 stage stage, maximal linear, sequence generators that are mod-two added to form a new code, The Gold code. This Gold code is then mod-two added with the selected data stream. This resulting digital signal is transferred out at one-half rate by two D flip-flops that are quadrature clocked. This signal, out of each flip-flop, is therefore a double bit length signal consisting of alternate bits from the composite Gold code and data signal which are quadrature clocked. These signals represent the quadrature vector, of the code, at half rate, because the code run length is an odd number (8191 bits).

These two orthogonal code streams, that are quadrature clocked are then used to biphase modulate the two 70 MHz quadrature phased carriers. The output of the biphase modulators are equally summed, and amplified by on-off controlled wideband 70 MHz amplifier with an output level greater than 0 dBm at 50 ohms. This wideband amplifier gate signal is the transmit signal, so when the transmit signal is activated, via the mike button front panel switch or remote barrier strip signal, the RF output is present. The 70 MHz carrier signal comes from a VCO that is adjustable via the front panel doppler potentiometer.

This system has 8192 possible codes, which are selected via five octal switches on the front panel. The first four switches counting from right to left, when looking at the front of the unit, have eight positions and the last switch (extreme left switch) has two positions, which allows any 13 bit binary number to be obtained. The two position switch is used to set the initial state of one flip-flop to a logic one or logic zero. The remaining switches each set the state for three flip-flops. To illustrate, when the switch is in the zero position, it represents the binary number 000 or a logic zero is instated into three flip-flops. When the switch is in the seven position, a binary logic 111 or a logic one is instated into the three flip-flops. Below is the octal to binary table up to octal seven.

Switch Position (Octal Number)	Flip-Flop States (Binary Number)
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Consider a code number from the switches and determine the (I. C.) initial conditions vector for the 13 stage coder. Consider code 12367. The Octal 1 equals binary 001; the Octal 2 equals 010, the Octal 3 equals binary 011, the Octal 6 equals binary 110, and the Octal 7 equals binary 111 -- therefore, the (I. C.) vector is 001, 010, 011, 110, 111.

Next, let us consider how the (I. C.) initial conditions vector is used to generate a new Gold code. The Gold code was generated by modulo-two addition of two equal length maximal linear sequence generators, whose characteristic equations are preferred pairs. To generate a new code in this system, the phase difference between the two codes is represented by the code number selected. What happens is everytime a predetermined code vector and load command occurs, one coder is cross-injected with the number stored in the code select switches and the second coder is set to its "all ones" vector state. The load command is generated by pressing the prep button, or the system goes through a "standby" to transmit transition.

Now consider the relationship between the coder clock and run length rate and phase to the data or voice clock rates and phase. Let us first note that when frequencies are synthesized by division, the resulting subharmonic can take on all n phases (division by n). But, when frequencies are synthesized by multiplication, the resulting subharmonic can take on only one phase. This result is the punch line to the approach used to generate phase and frequency coherent conditions for the data and voice clock rates relative to the PN code rates. The coder code output rate is 1.2285 MHz with a run length of 8191 bits, which results in a code period rate of 150 Hz. From the above information we can conclude that each code vector occurs at a 150 Hz rate or spectral lines spacing of 150 Hz.

To obtain a stable phase coherent data clock, the "all ones" vector is first extracted from one of the two internal coders. This "all ones" vector is then multiplied up to 9600, 2400, or 1200 Hz to give us a PHASE and frequency locked data or PDM clock to the PN code run length rate. In summary, to avoid the phase ambiguity problem when generating data and voice encoding clocks, that are at lower rates than the PN code bit rate, we multiply the code run length rate up. This requires the code run length rate to be an integer multiple of the data and voice clocks. For a code run length rate of 150 Hz and a 13 stage coder (8191 bits), we require a code bit rate (clock) of 8191 x 150 or 1228500 Hz.

As stated above, this unit accepts digital data at 1200 or 2400 bps, or audio signals via the mike, or front panel jack. The digital data is differentially encoded and the audio is suppressed clock pulse duration modulation (SCPDM) encoded. The algorithm for differential encoding is if the data bit is in a logic one state, change the state of the data bit out. If the data bit is in a logic zero state, then do not change the state of the data bit out. The SCPDM encoding process consists of:

a. Sampling the magnitude of the analog input at a give rate (9600 Hz for this system).

b. Convert each sampled magnitude signal to a pulse whose width is directly proportional to the magnitude (PDM).

c. Convert the PDM signal to SCPDM. This is equivalent to removing the reference edge of the PDM signal. Now, the reference edges is always of the same sign and occurs at the start of each bit interval. Therefore, by inverting alternate bit intervals, the reference edge is removed. In this system, this conversion

is implemented by the module-two addition of the PDM signal with a synchronous half rate clock (9600/2). The SCPDM processor also processes the analog (audio) signal prior to the SCPDM encoding. The audio input signal is AGC'd, pre-emphasized, and conditioned for speech usage. A more detail consideration of PDM encoding follows:

The PDM modulator generates an output pulse whose time duration is proportional to a sampled analog (audio) voltage. A block diagram of the PDM modulator is shown in figure 1. The audio conditioner section consists of a pre-emphasis circuit which increases the gain at 6 dB per octave between 600 Hz and 2.5 kHz.

The pre-emphasized audio is fed to an AGC amplifier, from which the signal is fed to a speech compressor-clipper. The speech compressor output is then coupled through a 2.5 kHz low pass filter having a 5 pole Legendre response with the 3 dB frequency at 2630 Hz.

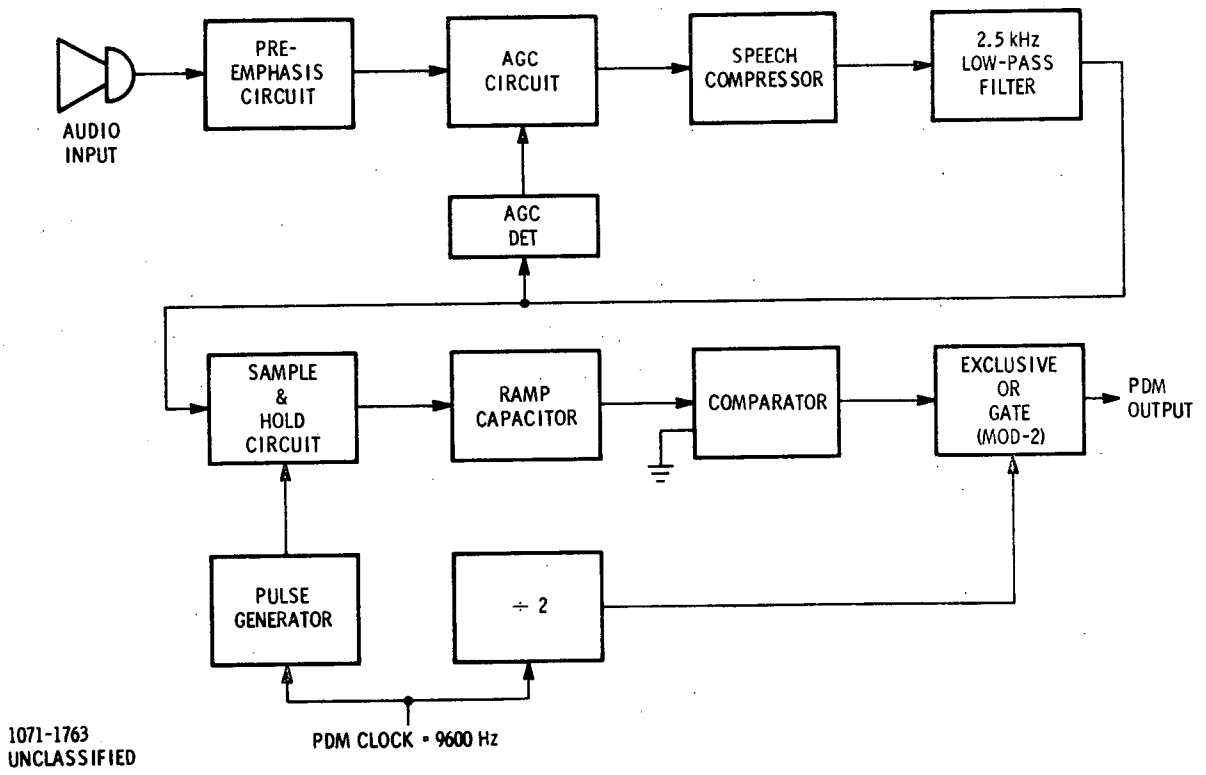


Figure 3-2. Transmitter PDM Modulator PDM Block Diagram

The maximum signal out of the low pass filter is 4.0 volts peak-to-peak centered at - 2.0 Vdc. This - 2 Vdc offset is required for proper PDM modulator operation.

The conditioned audio signal then drives a sample and integrate circuit. Than is, the audio is sampled at a 9.6 kHz rate; the samples being applied to a capacitor, which is also driven by a constant current source. Since the conditioned audio signal is always between 0 and -4 volts, the audio samples always result in negative voltages between 0 and -4 volts on the capacitor. The constant current source then pulls the capacitor voltage back above ground. A voltage comparator connected to the capacitor then changes state each time the voltage crosses zero. As a result, the time interval between negative and positive zero crossings is a linear function of the sampled input signal.

The output from the comparator is then a pulse duration modulated (PDM) 9.6 kHz subcarrier. Since the output of the audio conditioner is biased at - 2 Vdc, the comparator output will be a square wave if no audio is present.

The leading edge of the PDM subcarrier contains no information because it is always fixed in time. It is removed by modulo-two addition of a 4.8 kHz square wave with the 9.6 kHz PDM subcarrier. The result is a suppressed carrier PDM signal. Figure 2-3 shows the waveform at significant points in the PDM modulator.

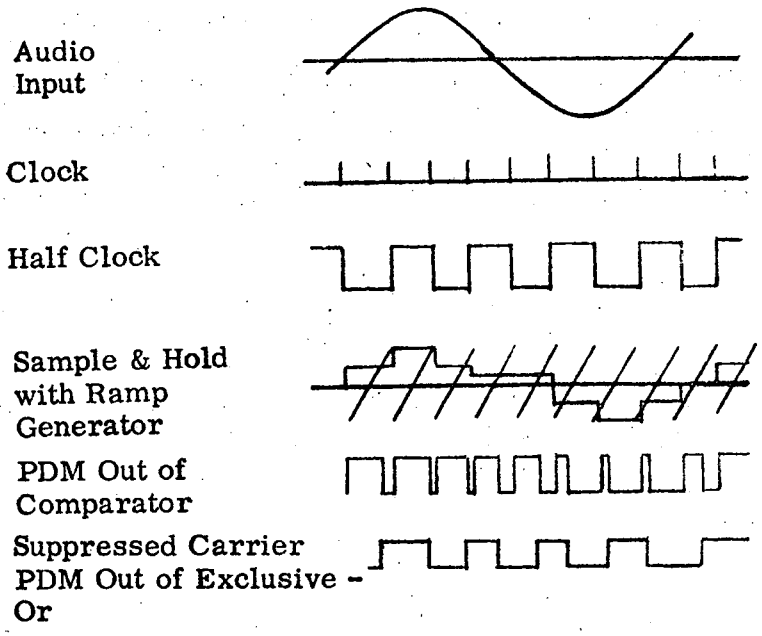


Figure 3-3. PDM Modulator Waveforms

3.3 MX-291 SYSTEM DESCRIPTION

There are three simplified block diagrams in this report of the MX-291 receiver. Figure 3-4 emphasizes an overview functional block diagram. Figure 3-5 emphasizes system implementation and location of functional blocks. Figure 4-18 connects Figure 3-5 to the actual signal routings and interface connections. The MX-291 PN receiver performs the inverse functions of the PN transmitter MX-290, by accepting the pseudonoise (PN) signal centered at 70 MHz and recovering the original information.

This system must first acquire code correlation before it can demodulate the information. This first step, of seeking code correlation, is referred to as the search process or sequence. Now, after it has acquired code correlation, it must maintain code correlation so that the information may be demodulated. To maintain code correlation the receiver's coder tracks the received code (transmit code) via a phase lock loop (PLL). The code tracking technique used by this system is referred to as the τ jitter or τ dither method. What happens is that after the receiver has acquired code correlation (sync) it then goes into the τ dither (tracking) mode of operation. The τ dither operation generates an incremental phase shift (fraction of a bit shift) on its own code at a given rate and uses this error, lack-of-correlation, signal to correct and maintain sync. In detail, this τ dither approach takes advantage of two properties of its autocorrelation functions: (1) $R(0) \geq R(\tau)$ and (2) $R(\tau) = R(-\tau)$. For the functions used here R(0) is greater than $R(\tau)$. Now, by τ shifting the code phase to the left, then to the right, by a fraction of a bit from R(0), and recording the difference as an error control signal $R(\tau) - R(-\tau)$. But, from the properties of the auto-correlation function $R(\tau) - R(-\tau)$ equals $R(\tau) - R(\tau) = 0$, or the error control signal is zero.

If we shift from R(0) and then do the incremental operation we will generate a difference or an error signal. This error signal is then used to set the code back to the in-phase, full-correlation condition. In this system a constant rate change in τ is used which is 7500 Hz. Also, by phase detection of this 7500 Hz rate τ signal, it is possible to determine what side of R(0) peak correlation, the receiver's code is. To summarize, the τ dither code tracking process uses the properties of the codes auto-correlation function to generate a control signal via a phase jitter. Also, by knowing what sign was assigned to the jitter it is possible to determine what side of R(0), no phase error or peak-correlation condition, the receiver's coder is located. With the τ jitter concept in mind and from figure 3-4 the ±0.2 bit (τ jitter) circuitry has three inputs: (1) the coder clock (VCO), (2) sync decision circuitry, and (3) the 7.5 kHz oscillator. Now, when a sync decision is made by the sync decision block it allows

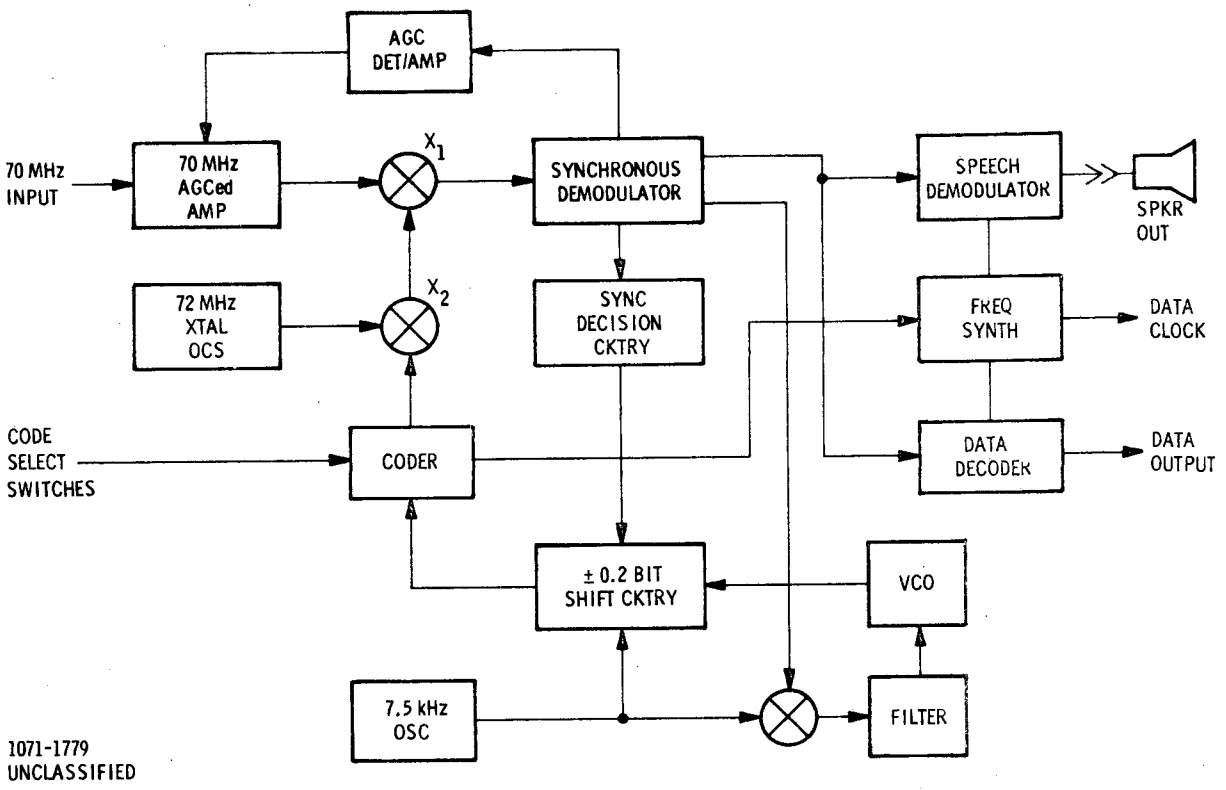


Figure 3-4. MX-291 Receiver Unit Block Diagram

the 7500 Hz oscillator signal to shift the coder VCO by ±.2 bits at a 7500 Hz rate which in turn causes a variation in the output of the synchronous demodulator if it is not fully correlated. This signal is then phase detected by the multiplier shown in figure 3-4. The output of the phase detector is then filtered and used as the control voltage to the code clock VCO of figure 3-4.

Also, when the receiver is in the tracking mode it must demodulate the data. The signal out of the correlator mixer is a PSK encoded carrier centered at 2 MHz plus or minus all the off-set frequencies caused by doppler shift and oscillator off-sets. A Costas loop is used to track and to coherently demodulate this PSK signal. The inphase and quadrature signals from the Costas loop are processed to extract the data, τ jitter signal, AGC signal and code correlation signal. First consider the signals required when the system has acquired code synchronization and the costas loop is locked to the incoming signal and the system is in the tracking mode. The inphase and quadrature signal are first filtered by a RC low pass filter equal to the selected data rate and we call them the (I) and (Q) signals. These I and Q signals are converted to binary signals via a hard decision network (Schmitt), and called $\_/\overline{I}$ and $\_/\overline{Q}$. The $\_/\overline{I}$ and $\_/\overline{Q}$ signal in conjunction with their own I and Q signal are multiplied to form the absolute value

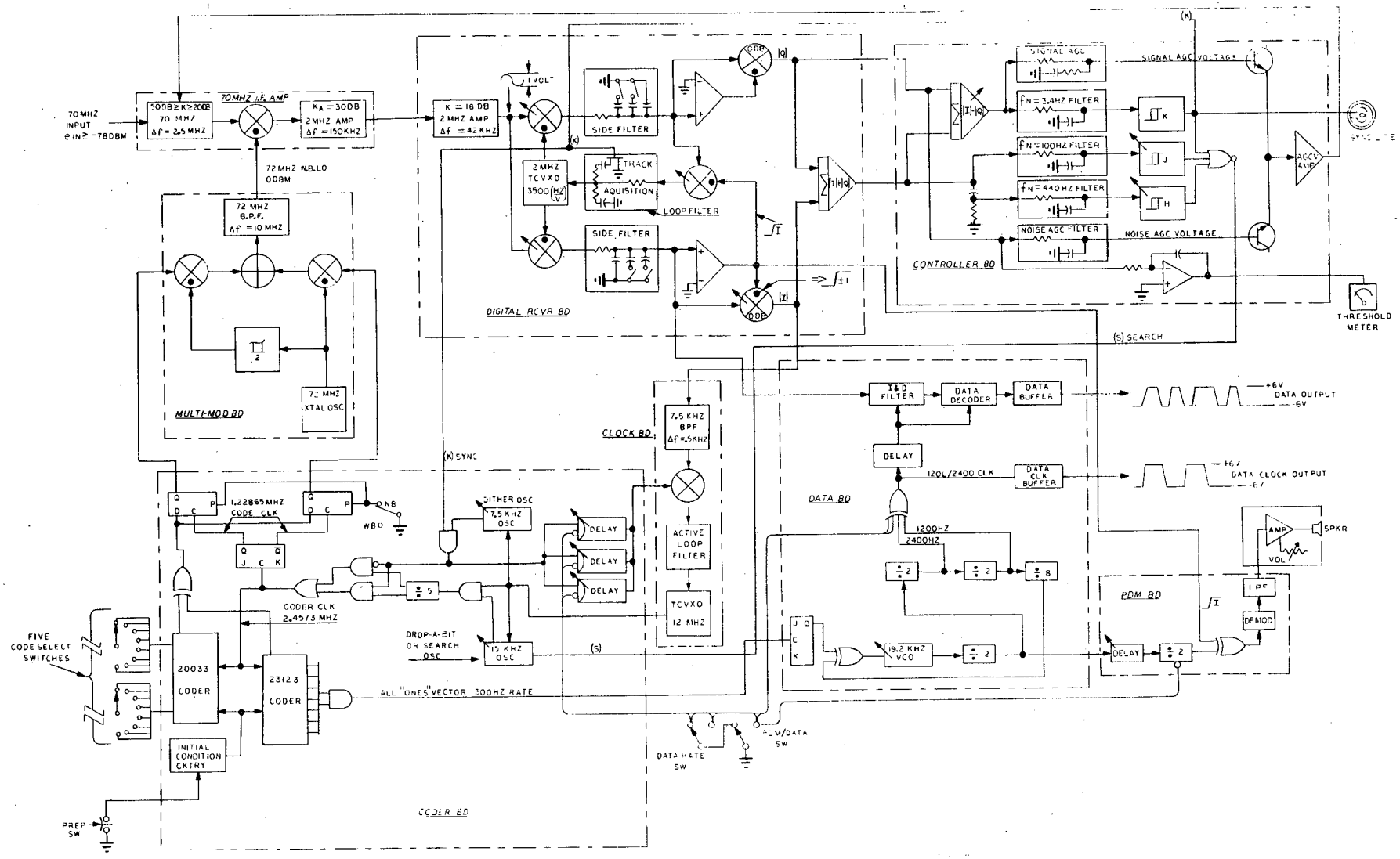


Figure 3-5. MX-291 Receiver Data System Block Diagram

or magnitude of I and Q called magnitude I and magnitude Q symbolically $|I|$ and $|Q|$. NOTE: consider I and Q in expotential form (complex functions) and if $\_/\overline{I}$ and $\_/\overline{Q}$ has a modulas of one or minus one then when $\_/\overline{I}$ and $\_/\overline{Q}$ is multiplied with I or Q the result would be a modulas of ±I or ±Q and, the argument would be the sum of their arguments. This system uses linear or chopper multiplier circuits; therefore, the above condition applies. The $\_/\overline{I}$ signal is processed to acquire the data signal. For digital data the $\_/\overline{I}$ signal is: (1) filtered by an integrate and dump filter (I&D), (2) then converted to a binary signal by a hard decision (Schmitt) network; (3) then differentially decoded by the mod-two addition of a two-bit static shift register.

For the audio signal the $\_/\overline{I}$ signal (SCPDM) is first mod-two added with a 9600 Hz properly phase clock to form the PDM signal. This PDM signal is converted to a PAM signal, deemphasized and filtered by a 2500 Hz low pass filter resulting in the audio signal..

The $|I|$ and the $|Q|$ signals are subtracted to form $|I| - |Q|$ and low pass filtered, and used as signal AGC. Now, the $|I|$ signal is stripped of the PSK signal but, it has the τ dither (an AM signal) signal on it and is used to acquire the τ dither control signal, as explained before.

When the MX-291 is not in sync the $|Q|$ is low pass filtered to form the noise AGC signal. The $|I|$ is summed with the $|Q|$ to form $|I| + |Q|$ which is the absolute value (magnitude) of the correlator output (full-wave rectification). This signal is processed by two low pass filters followed by a hard decision (Schmitt) network and used to indicate that a possible code correlation condition occurred.

The objective of the dual sync decision circuitry, H and J, is to minimize time to obtain code correlation with the constraint of 90% probability of detection per pass. Also, a third and final sync decision is acquired by a low pass filter-Schmitt operation on $|I| - |Q|$ signal. The H and J sync decision does not require the Costas loop to be in lock, because $|I| + |Q|$ is equal to the correlator output magnitude. The K sync decision is acquired by processing $|I| - |Q|$ which does require the Costas loop to be in lock. Therefore, the final sync decision K means that code correlation has been obtained and the Costas loop is in sync.

All the sync decision signals, H, J, and K are logic NORed to form the search signal (S), or

$$S = \overline{(H + J + K)} - \overline{H} \cdot \overline{J} \cdot \overline{K} \cdot \text{Search}$$

signal (S) is the search command signal which is true when the system is searching for code correlation. The H, J, and K circuits consists of Schmitts with specific hysterises requirements. The H Schmitt with its specified hysterises and level requirements will cause a 30% reduction in the search rate when operating in a noise environment. The J Schmitt network is set for a 10% stop search requirement when searching noise only.

Now, let us consider how this system acquires code correlation or sync. As stated above, when this system is in sync the correlator mixer output is a PSK signal (a 2 MHz carrier biphase modulated with the data) or a CW signal (2 MHz carrier) if no data is being transmitted. Prior to code correlation the correlator mixer output signal bandwidth consists of the sum of the input signal bandwidth and the local reference bandwidth. The local reference bandwidth has the PN Sin X/X envelope, and with a clock of 1.2 MHz the nulls occur at ±1.2 MHz, which is equivalent in general to a uniform bandwidth of 1.2 MHz. Therefore, if a CW signal enters the correlator it is transformed or spread to the PN 1.2 MHz bandwidth (61 dB). Now the sync decision filters that process the correlator output have a noise bandwidth of 690 Hz (28.4 dB) and 159 Hz (22 dB). Therefore, when correlation occurs, the inband signal energy increases and the filter-Schmitt sync decision networks make a sync decision which stops the search process, until all sync decision networks state a no sync condition.

This system uses the sliding correlator method to acquire code sync. Therefore, the coders clock frequency must be reduced so that the local reference code runs at a slower rate than the transmit code, or the local PN code slides back into correlation with the transmitted code. In this system a fixed 7500 Hz oscillator is used to phase shift the coder clock in increments of minus two tenths a bit at a 7500 Hz rate, if S, the search signal is true. This results in a raw search rate of 1500 Hz, and an effective search rate of 1000 Hz. Remember, H has a false alarm rate of 30%, so 2/3 x 1500 Hz = 1000 Hz is called the effective search rate. The PN sequence has a run length of 8191 bits, which means that it takes 8 seconds to make one pass of the sequence.

Figure 3-4 is a simplified block diagram of the MX-291. In figure 3-4 mixer X2 generates the 72 MHz centered SQPM signal from the 72 MHz oscillator and the Gold code from the coder. The output of X2 is mixed with the 70 MHz AGC, input signal to X_1, which is the correlator mixer. The synchronous demodulator processes the correlator mixer (X_1) output to form I, $|I|\_/\overline{I}$, Q, $|Q|$, $\_/\overline{Q}$ and $|I| \pm |Q|$ signals. The $|Q|$ and $|I| - |Q|$ go to the AGC det/amp block to form the AGC control voltage.

The $|I| + |Q|$ and $|I| - |Q|$ go to the sync decision circuitry to form the search signal (S). The $|I|$ signal goes to the 7.5 kHz phase detector to obtain the τ dither control signal. The $\overline{I}$ signal goes to the speech and digital data decoder to extract digital data or speech.

The τ dither control signal from the 7500 Hz phase detector is filtered and used to control the coder VCO. The coder VCO output signal is phase shifted alternately by ±.2 bit at a 7500 Hz rated OR -.1 bit at a 15 kHz rate depending upon the state of S, the search signal. If S is logic true then the system is in the search mode; therefore, phase shift the VCO signal by -.1 bit at 15 kHz rate. The output of the shift circuitry, the phase shifted coder clock, goes to the coder as the coder clock signal. The coder is code programmed by the code select switches to generate the required Gold code and its "all ones" vector. The "all ones" vector occurs at a 150 Hz rate which is transferred to the frequency synthesizer. The Gold code is sent to X_2 the SQPM mixer described before. The frequency synthesizer generates the data clocks by multiplying the 150 Hz rate "all ones" vector. The speech demodulator processes the $\overline{I}$ to form the audio output signal. The data decoder takes $\overline{I}$ and with the 1200 Hz or 2400 Hz clock obtains the digital data output signal. The digital data out is obtained from $\overline{I}$ by integrate and dump filtering followed by a binary decision on the filter output, then differentially decoding.

In figure 3-5, the multi-mod board contains the SQPM modulator and the 72 MHz crystal oscillator, which is phase shifted by $\pi/2$ radian or 90 degree to form two quadrature carrier signals. These two carrier signals are each biphase modulated, with two quadrature clocked and time displaced, versions of the Gold code from the coder board. The output of these two biphase modulators are equally summed and amplified to form the SQPM signal at a 0 dBm level. This SQPM signal is used as the local reference signal into the correlator mixer located in the 70 MHz IF can.

The 70 MHz input signal is AGC, to set the signal level into the correlator at -38 dBm. The correlator mixer is a double balanced mixer with a conversion loss of less than 7 dB given a signal output of -45 dBm. The 2 MHz centered signal out of the correlator is amplified by a single tuned bandpass amplifier whose maximum gain is 30 dB and has a 3 dB bandwidth of 150 kHz (51.75 dB) or a noise bandwidth of 53.75 dB. When the system is sync, the 2 MHz centered signal is at a -15 dBm level, which is also the output of the 70 MHz IF can.

The digital receiver board takes the 2 MHz centered signal from the 70 MHz IF can and first amplifies it by 18 dB with a single tuned bandpass amplifier whose noise bandwidth is 48 dB. The correlated signal out of this amplifier is one volt peak-to-peak (1 volt Pk-Pk) and it sets the gain constant of the phase detectors of the Costas loop. Also, this unit is DC coupled from this point on; therefore, DC off-sets must be accounted for and/or adjusted out. The processing gain up to this point approaches 13 dB (61 dB - 48 dB = 13 dB. This means, for an input signal to interference ratio (S/I) of -19 dB the signal to interference at this point would be -19 dB + 13 dB = -6 dB or the rms noise voltage is .707 volts. The one volt peak-to-peak is multiplied by the Costas loop 2 MHz VCO in the Costas loop inphase and quadrature phase signals. These two signals are each filtered by a simple low pass RC filter to form what is called the I and Q signal. From figure 3-5, we can see that there are three selectable RC filters. The 3 dB frequencies are 9600 Hz, 2400 Hz and 1200 Hz. The 1200 Hz filter is used prior to tracking, during acquisition, and the 1200 Hz digital data rate mode. The 2400 Hz and 9600 Hz filters are used during the 2400 Hz digital data tracking and 9600 Hz SQPDM speech tracking modes respectively. I and Q are Schmitted to form $\_/\overline{I}$ and $\_/\overline{I}$ and $\_/\overline{Q}$. I's multiplied with $\_/\overline{I}$ and Q is multiplied with $\_/\overline{Q}$ to form the absolute value or magnitude of I and Q which are also called the absolute value of I and Q, symbolically $|I|$ and $|Q|$.$|Q|$is also multiplied by $\_/\overline{I}$ which is the third multiplier of the Costas loop to form the unfiltered VCO control voltage. This signal is filtered by Costas loop filter and then applied to the Costas loop VCO. This system has two loop filters, one for acquisition and one for tracking. When the final sync decision (K) has been made, the tracking filter is used, and prior to this the system was searching for code correlation; therefore, the acquisition filter is used. The $|I|$ and $|Q|$ are equally summed, by an OPA summer to form the $|I| + |Q|$ signal, which is the magnitude of the correlator output. Note, that $|I| + |Q|$ signal is not related to the status of the Costas loop, where $|I|$ and $|Q|$ etc., are dependent functions.

The controller takes the $|I| + |Q|$ and $|Q|$ signals from the digital receiver and forms the difference between the magnitude of I and the magnitude of Q or, $|I| - |Q|$ signal. When the system is searching for code correlation $|I| - |Q|$ signal is zero volts, and $|Q|$ represents one of the two quadrature magnitude components of the uncorrelated correlator outputs. When the system acquires code correlation, and the Costas loop locks-up, and the system goes to the tracking mode then $|Q|$ goes toward zero and the $|I| - |Q|$ approaches the $|I|$. Now, $|I|$ is the magnitude of the coherent inphase vector out of the correlator, or the magnitude of the coherent correlated

signal. These properties of |Q|and | I |- |Q| are used to form the AGC control voltage. The |Q|and | I |- |Q| signals are filtered, and the most positive of these two filtered signals is compared to a reference voltage then used as the AGC control signal. Therefore, the AGC control signal is |Q| during acquisition and | I | - |Q| during tracking. Also, | I | + | Q| and | I | - |Q| are also processed on the controller board to form S and K the sync decision signal. This is accomplished by low pass filters followed by Schmitts with preset hysterises and levels.

| I | signal is processed to obtain the τ dither signal when the system is in sync. The | I | signal is used to obtain the τ dither signal because the biphase modulated data on I is removed when the magnitude of I is formed, but the amplitude modulated signal caused by τ dither is not removed. | I | signal goes to the clock board where the τ dither error control signal is obtained and applied to the coder clock VCO. From figure 3-5 the | I | signal is first filtered by a 7500 Hz centered 500 Hz bandpass filter. The filter output signal is then multiplied with the properly phased 7500 Hz dither clock from the coder board. This multiplier is the phase detector of the coder clock tracking phase loop, which is then filtered by the active loop filter. The loop filter output is applied to the 12 MHz TCVCXO, which is also located on the clock board.

The data board takes the 300 Hz rate "all ones" vector from the coder board and use a phse lock loop to multiply this signal up to 19.2 kHz. The 19.2 kHz clock is then divided down to form the required data clock rates of 9600 Hz, 2400 Hz and 1200 Hz. The 9600 Hz clock goes to the PDM board, and the required digital data clock is buffered out to meet MIL-STD-188B, at ±6 volt signal. This signal is also delayed to account for difference in delay between the correlated code phase and the demodulated data at I in the digital receiver board. This delayed digital clock signal is used as the digital data differential decoder clock, and it is shaped to form the dump pulse of the I and D filter. The I signal into the data board is first filtered by an integrate and dump (I and D) filter set for the selected digital data rate. The output of this I and D filter is converted to a binary signal by a hard decision Schmitt that assigns a logic one to all signals above zero volts and a logic zero to all signals below zero volts. This digital differentially encoded signal is then decoded by mod-two addition of the outputs of a two-bit shift register whose input is the encoded data. This decoded digital data signal is then buffered out via MIL-STD-188B as the DATA OUTPUT signal.

When this system is in the PDM mode, $\_/\overline{I}$ signal from the digital receiver board is the SCPDM signal that is demodulated by the PDM board to form the AUDIO OUTPUT signal. The PDM board takes the 9600 Hz clock and divides it by two and then mod-two adds this signal with $\_/\overline{I}$ to form the PDM signal. This PDM signal is demodulated by converting the PDM signal to a PAM signal followed by a sample and hold then low pass filtered to form the audio signal. The low pass filtering consists of deemphasis followed by a 2500 Hz five pole Legendre filter.

The coder board derives the preselected Gold code, and phase shifts this code plus and minus two tenths or minus one tenth of a bit depending upon if the system is searching or tracking. When (S), the search signal, is true the code is phase shifted by minus one tenth of a bit at a 15 kHz rate. When (K), the sync signal is true, the coder is alternately phase shifted plus and minus two tenths of a bit at a 7500 Hz rate, to generate the τ dither tracking control signal. The 12 MHz clock oscillator signal is logic AND gated with a synchronized 15 kHz oscillator to inhibit one 12 MHz clock pulse per 15 kHz clock pulse. The output of the AND gate is divided by five and ten to form the clocks required to form the Gold codes. The divide by ten clock is used as the output code clock; therefore, a one bit shift at 12 MHz represents one tenth of a bit shift at 1.2 MHz. To generate the τ dither signal, the 12 MHz clock is divided by five and two phases of this divider is alternately selected at a 7500 Hz to form the 2.4 MHz coder clock. This 2.4 MHz clock is then divided by two to form the code output clock. The Gold code is formed by the mod-two addition of two preferred pairs, 13 stage PN code generators. The octal number of the characteristic equation of the two pairs are 20033 and 23123. To generate new codes, the 20033 coder initial conditions is set by the front panel code select switches, and the 23123 coder is initialized to its all ones state. Therefore, the basic concept of new codes here is formed by changing the initial condition of a given difference equation that is multiplied by a second difference equation of same order and fixed initial conditions. When the PREP$\overline{\text{P}}$ button is pressed, the selected code is initiated by the generation of initial condition signals, which crossinjects the prescribed requirements into the two coders. The 20033 coder is mod-two added with the 23123 coder to form what has been defined as the Gold code. This 2.4 MHz clock rate Gold code is then transferred out two lines at a 1.2 MHz rate by alternate clocking the 2.4 MHz code into two D flip-flops, which also extends a bit interval to a two bit length interval. The output of these two flip-flops are quadrature clock versions of the same Gold code displaced by exactly one-half its run length (8191/2). The multi-mod board uses these two codes to form the 72 MHz SQPM signal.

3.4 SUMMARY SPECIFICATIONS FOR MX-290 AND MX-291

3.4.1 GENERAL

Item	Required
AC Power Input:	
Frequency:	57 - 440 Hz
Voltage:	110 ± 15 volts
Carrier Interface Frequency:	70 MHz
Modulation (Composite Signal):	SQPM
Digital Data :	DPSK
Voice :	SCPDM
Code Clock Frequency :	1.228 MHz
Code Length:	8191 bits
Addresses :	8192
Code Repeater Frequency :	150 Hz
Digital Data Interface :	MIL-STD-188B

3.4.2 SPECIFICATIONS OF MX-290(TRANSMITTER)

	Required	Measured
RF Output:		
Carrier Frequency:	70 MHz	
Power Output :	0 dBm	+6 dBm
Bandwidth (Null-Null):	2.4 MHz	
Data Input Frequencies:		
Digital :	1200 Hz or 2400 Hz	
Audio (mike input) :	(300 - 2500) Hz	
Digital Data Clocks :	1200/2400 Hz	
Carrier Frequency Control (DOPPLER):	± 5 kHz	

	Required	Measured
AC Power Input:	60 watts	
DC Power (Internal):		

Voltage	Amps	
	Available	Measured
+12	0.6 A	0.07 A
+5	3.0 A	0.53 A
-12	0.6 A	0.10 A

3.4.3 SPECIFICATIONS OF MX-291 (RECEIVER)

Item	Required	Measured
RF Input:		
Carrier Frequency:	70 MHz	
Sensitivity:	≤-78 dBm	≤-80 dBm
Dynamic Range:		-80 dBm to -50 dBm
Data Output:		
Digital:	1200 Hz or 2400 Hz	
Audio (Speaker):		
Power:	0 dBm	>10 dBm
Frequency Response (+1 db, -3 db)	300 - 2500 Hz	300 - 2500 Hz
Digital Data Clocks :	1200 Hz or 2400 Hz	
Tracking Threshold (Data):	15 db	≥22 db
(Voice):	13	≥22 db
Aquisition (S/N) db in		
(Data):	-13 db	-15 db
(Voice):	-10 db	-15 db

	Required	Measured
Audio Output (S/N) db	14 db	17 db
for (S/N) db in of	-11 db	-11 db
Data Error Rate (10^{-5})		
1200 Hz (S/N) db in	-15 db	-20 db (2×10^{-5})
2400 Hz (S/N) db in	-13 db	-17 db (2.2×10^{-5})
AC Power Input:	60 watts	

DC Power (Internal)

Voltage	Amps	
	Available	Measured
+12 V	0.6 A	0.23 A
-12 V	0.6 A	0.25 A
+5 V	3.0 A	1.07 A

SECTION IV

SYSTEM IMPLEMENTATION

4.1 MX-290 TRANSMITTER DESCRIPTION

4.1.1 INTRODUCTION

The systems concept of the MX-290 unit is described in the preceding section. The objective of this section is to take this systems concept and show how it was implemented.

For the breakdown of the transmitter to the individual subunits refer to the block diagram figure 4-1. As seen in this block diagram, the transmitter unit consists of four circuit boards, two power supplies, a front control panel, and a rear signal access panel. All of these subunits are contained in a portable cabinet with all the required interconnecting wires and cables.

a. Controller board (J101)
b. Coder board (J102)
c. Multi-mod board (J103)
d. PDM mod board (J104)

4.1.1.1 Coder Board

The coder board performs the following functions:

a. Generates one of 8192 codes pre-selected at the front panel code selector switches.

b. Mod-two adds a selected code with the encoded pre-selected data to form the composite signal.

c. Forms two quadrature clocked versions of the composite signal displaced with respect to each other by one-half the code run length.

d. Generates its own clock signal.

e. Generates the 150 Hz clock signal.

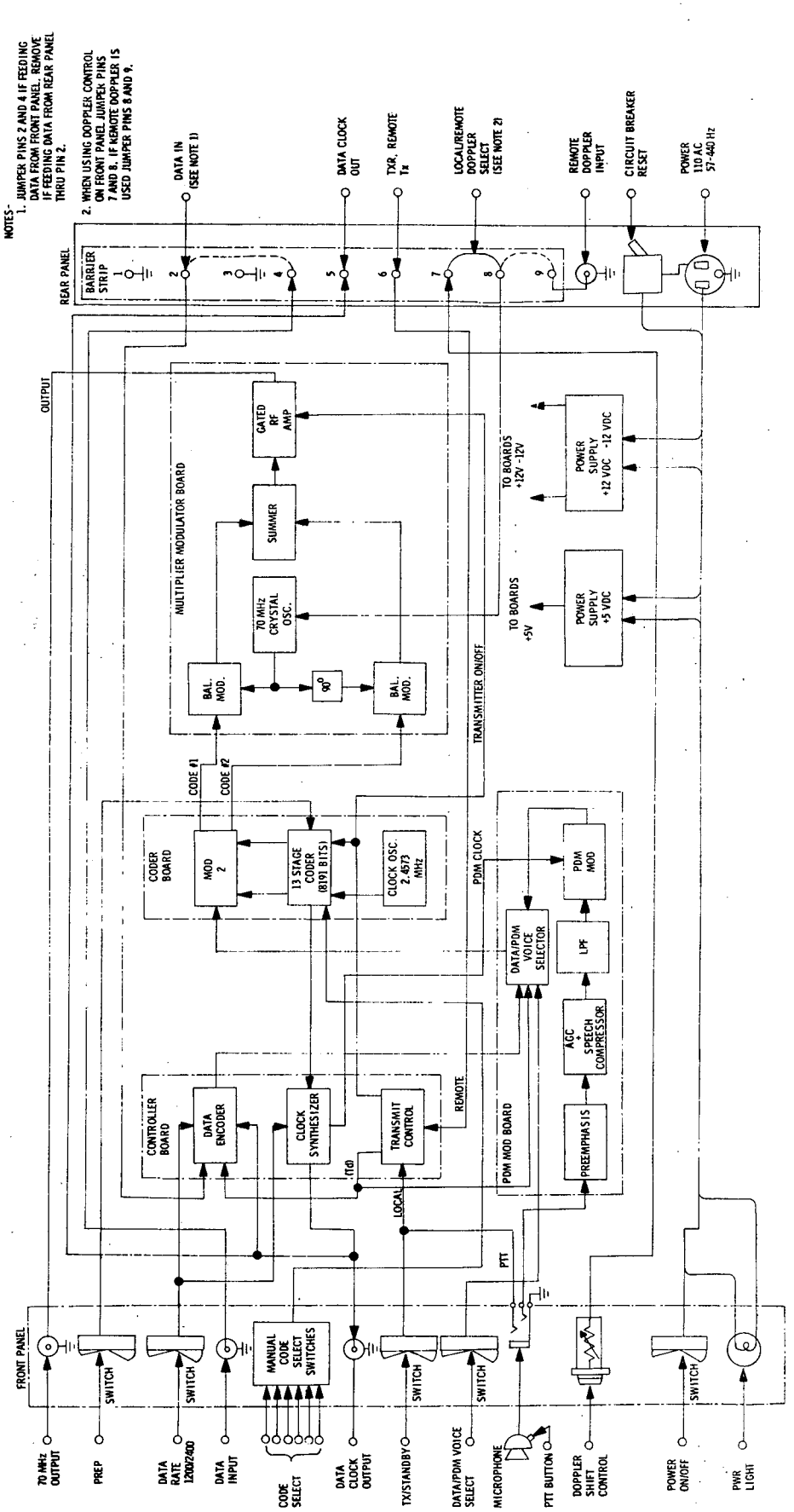


Figure 4-1. MX-290 Transmitter Block Diagram

4.1.1.2 Multiplier-Mod Board

The multiplier-mod board performs the following functions:

a. Generates the 70 MHz carrier signals via the front panel doppler pot or a signal into the assigned barrier strip terminal lug.

b. SQPM the above 70 MHz VCXO with the quadrature clocked digital signal from the coder.

c. Buffering and gating of the modulated signal to the output jack.

Two quadrature 70 MHz carrier signals are formed from the VCXO and each is first bi-phase modulated with their quadrature clocked orthogonal code streams and then summed. This modulated signal (SQPM) is then buffered to the 70 MHz output jack which is also gated on or off by the transmit control signal. The 70 MHz oscillator is voltage controllable, which can provide up to $\pm$ 5 kHz from its center frequency for the purpose of simulating carrier doppler shift.

4.1.1.3 Controller Board

The controller board performs the following functions:

a. Generates the transmitter ON/OFF control signal from either local or remote transmit control line input.

b. Generates the required data clock from the coder's "all ones" vector and supplies data clock to both front and rear panels. The required data clock rate is 1200 or 2400 or 9600 Hz depending upon data mode selected.

c. Accepts digital data input and differentially encodes the digital data.

When the local or remote transmit control line is grounded, a (T) transmit signal is generated, which is used to initiate the coder and gate the 70 MHz RF output on. Ten seconds after (T) a delayed signal (T_d) occurs which is used to inhibit data for the first ten seconds.

The controller board generates its data clock from the "all ones" vector (C_i) of the coder. The "all ones" vector (C_i) occurs at a 300 Hz rate, which is used as the reference input to a phase lock loop multiplier circuit to generate the 1200 Hz and 2400 Hz clock signals for digital data inputs and 9.6 kHz for PDM. The data rate switch on the front panel selects either one of the digital data clock rates. This clock signal is sent to the differential encoding circuit on this card, and also buffered to the front and rear panels. The 9,600 Hz clock signal is supplied internally to the PDM board only.

4.1.1.4 Tx PDM Conditioner Board

The Tx PDM conditioner performs the following functions:

a. Accept the audio signals from the microphone and process these signals into a form acceptable to the SCPDM encoder. This processing consists of pre-emphasis, gain control and speech compression and low pass filtering.

b. Accept the processed speech signals and convert the amplitude to suppressed clock pulse duration modulation. This function is performed by the PDM modulator block. The output of this block consists of binary amplitude (TTL), variable duration signals compatible for digital processing.

c. From ED2 signal, which is the selection command for either the SCPDM signal or the differentially encoded data signal. Signal ED2 goes to the coder.

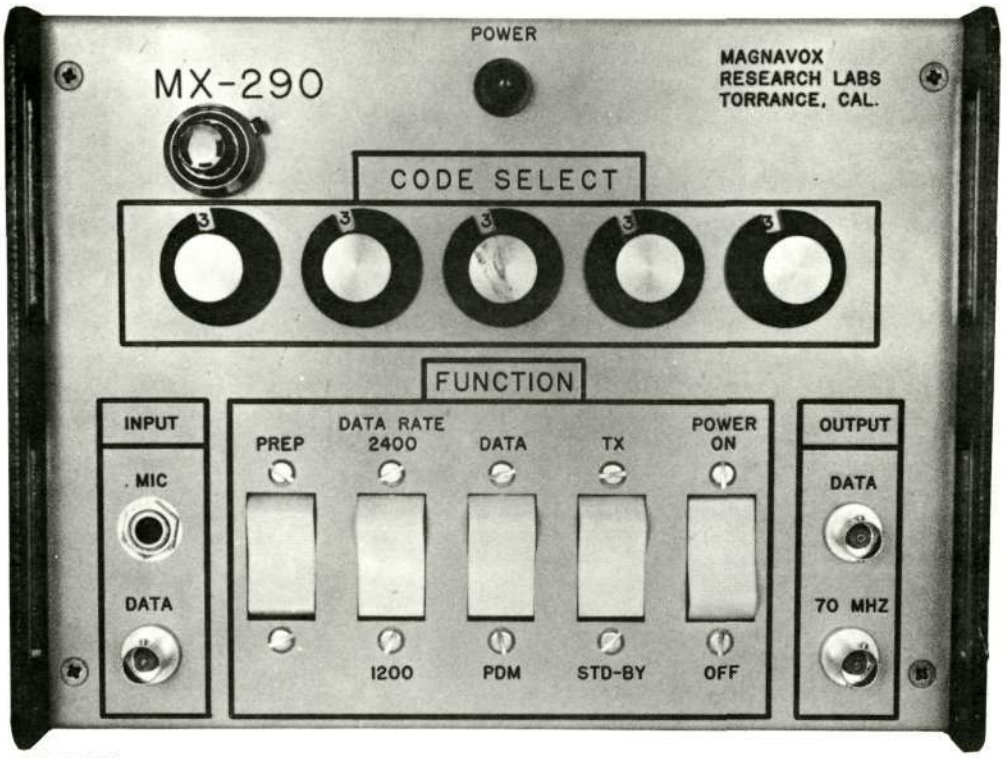
4.1.1.5 Front and Rear Panel

All of the operator controls for the transmitter are located on the front panel. As shown on figure 4-2, most of the controls are self-explanatory. However, a brief description of each switch and input-output connectors are presented in table 4-1. Refer also to the front panel subunit portion of the overall block diagram (figure 4-1).

The rear panel layout is shown in figure 4-3. As shown, the only interface connectors are the power plug, the barrier strip, and the external doppler simulated BNC. The function of various pins of the barrier strip and the interconnections with the remainder of the transmitter units are also explained in figure 4-3.

4.1.1.6 Multi-Mod Board (J101)

For the purpose of brevity, all boards described henceforth will be referred to by their corresponding connector numbers. For example, an alternate name for the Multi-Mod can be its connector call-out J101. Such nomenclature also allows identification of the card location in the card case. Note, that all one hundred series connectors are for the transmitter; the unit digit calls out board location in the card cage when counting from left to right. From this, it is seen that the multi-mod is the first board on the left in the transmitter card cage. Because the transmitter multi-mod board is identical to its receiver counterpart, except for a different oscillator, only one figure with callouts is shown in this report and it is the receiver multi-mod (J202).



971-1667
UNCLASSIFIED

Figure 4-2. MX-290 Front Panel Layout

Table 4-1. MX-290 Front Panel Control Descriptions

Item	Function
POWER ON/OFF Switch and indication	AC power ON/OFF Switch
TX/STD-BY Switch	Places the transmitter in either transmit or standby condition.
DATA/PDM Switch	Selects digital data or PDM mode of operation.
DATA RATE 2400/1200 Switch	Digital data rate select switch
PREP Switch	This switch is used to initialize coder states.
CODE SELECT Switches	The five code select switches are used to program to the coders to generate one of the available 8192 PN codes.
Input MIC Jack	For microphone input in voice mode.
Input DATA Connector	Allows digital data input when in digital data mode.

Table 4-1. MX-290 Front Panel Control Descriptions (Continued)

Item	Function
OUTPUT DATA Connector	Output from the digital data clock.
OUTPUT 70 MHz Connector	70 MHz SQPM modulated output.
Doppler Shift Potentiometer	This control, located on the upper left hand corner of the panel, provides for simulated carrier doppler shift of ±5 kHz.

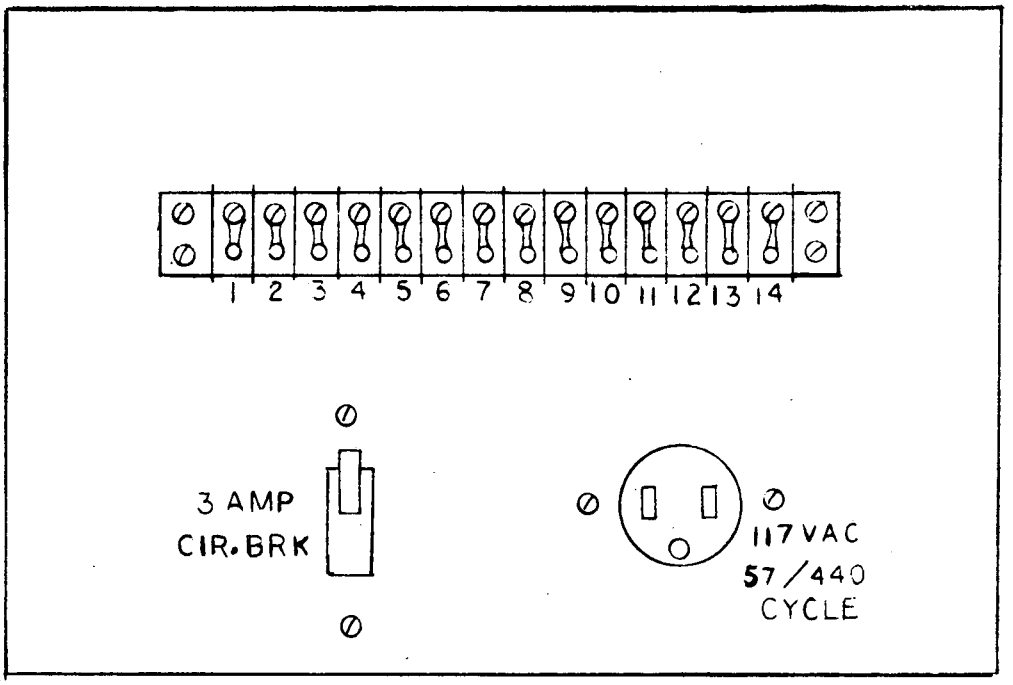
Figure 4-4 is a block diagram and 4-5 is the schematic diagram for (J101), i.e., the transmitter multi-mod board. This board generates the 70 MHz staggered quadriphase modulated (SQPM) signal from its internal VCXO and the two code stream inputs (code, $\overline{\text{code}}$). The 70 MHz output is on-off controlled by the "-12T" control signal.

The code and $\overline{\text{code}}$ signals, which are TTL logic level signals, enter at pins (9) and (7) and come from pins (C) and (2) located on the coder board J102. The transmit (12T) command signal enters at pin (3) and comes from the controller (J101), pin P. The 70 MHz output signal on pin (13) (J101-13) goes to (P4), the 70 MHz output BNC connector on the front panel. P4 output level is approximately +6 dBm.

The 70 MHz voltage controlled crystal oscillator (VCXO) control line enters at pin (A) and comes from the barrier strip located on the rear panel. To use the front panel doppler potentiometer for oscillator control voltage connect a jumper between pins 7 and 8 on the barrier strip.

The following description is related to figure 4-4 and 4-5. The 70 MHz VCXO sinusoidal signal is connected to a phase-splitter network consisting of Q1, L1, C5, C6, R5, and R6. The phase splitter's function is to form two 70 MHz output signals in quadrature.

These two quadrature-phased 70 MHz signals are then fed to their respective double balanced mixers. The mixers which are designated as X1 and X2 of figure 4-4 and T1 and T2 of figure 4-5, accept the two 70 MHz carriers and biphase modulate them with their respective code streams, i.e., code and $\overline{\text{code}}$. These two code streams are quadrature clocked versions of the same code displaced by exactly one half their run length. The outputs of the mixers are equally summed to form the staggered



CONNECTIONS ON BARRIER STRIP MX-291

*PIN 1. SAFETY GROUND

PIN 2. DATA CLOCK OUTPUT REMOTE

PIN 3. SHIELD GROUND

PIN 4. TD FRONT PANEL BNC DATA OUTPUT

PIN 5. DATA OUTPUT — SEE NOTE

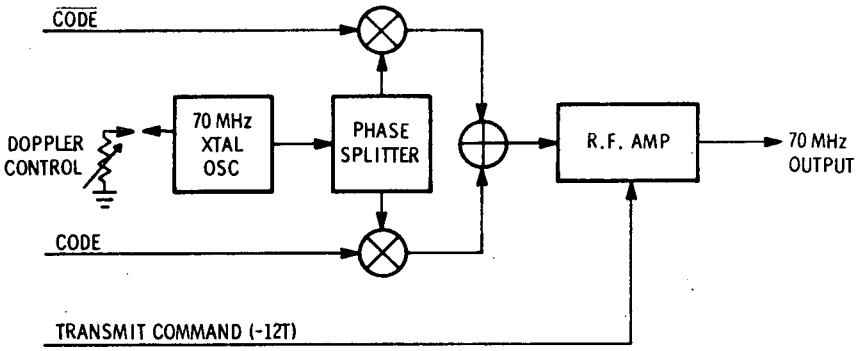
PIN 6. SHIELD GROUND

*PIN 1. LEFT SIDE WHEN FACING BACK PANEL

NOTE: TO USE DATA OUTPUT FROM FRONT PANEL BNC JUMPER PIN 4 and 5 TO TAKE DATA OUT FROM BACK PANEL USE PIN 5 and 6.

1071-1764
UNCLASSIFIED

Figure 4-3. Rear Panel Layout



1071-1766
UNCLASSIFIED

Figure 4-4. Block Diagram of MX-290 Multi-Mod Board (J101)

quadriphase modulated (SQPM) signal. This is accomplished by the summer as shown in figure 4-4 and by resistors R12, R13, and R14 in figure 4-5. R13 is a potentiometer which is adjusted for equal power from each balance modulator.

The SQPM signal is then amplified and buffered to an output power level of +6 dBm. This amplifier is gate controlled by the -12T signal from the controller. The function of this control signal is to gate on or off the 70 MHz output signal for transmit or STD-BY. This is accomplished by U1 shown in figure 4-5. When the 12T signal is at -12 volts, the 70 MHz SQPM signal is transferred to the output (on condition). When the -12T signal is above +1 volt the output RF is reduced to approximately -40 dBm (off condition).

4.1.1.7 Coder Board (J102)

The components for board J102 are assembled on a universal printed circuit board with magnetic wire for jumper connections of circuit elements. The 7400N series, in-line packaged, digital logic was used to implement these digital functions. For the following description, figures 4-6, 4-7, and 4-8 are used.

Purpose of J102

The purpose of J102 is to:

a. Generate one of the 8192 Gold codes, via the front panel code select switches.

b. Mod-two add the selected data with the selected Gold code.

c. Generate two phases of item (b) that are code phase shifted by one half its run length (8191/2) and quadrature clocked.

d. Extract the "all ones" vector from one of the coders which occurs once each code cycle.

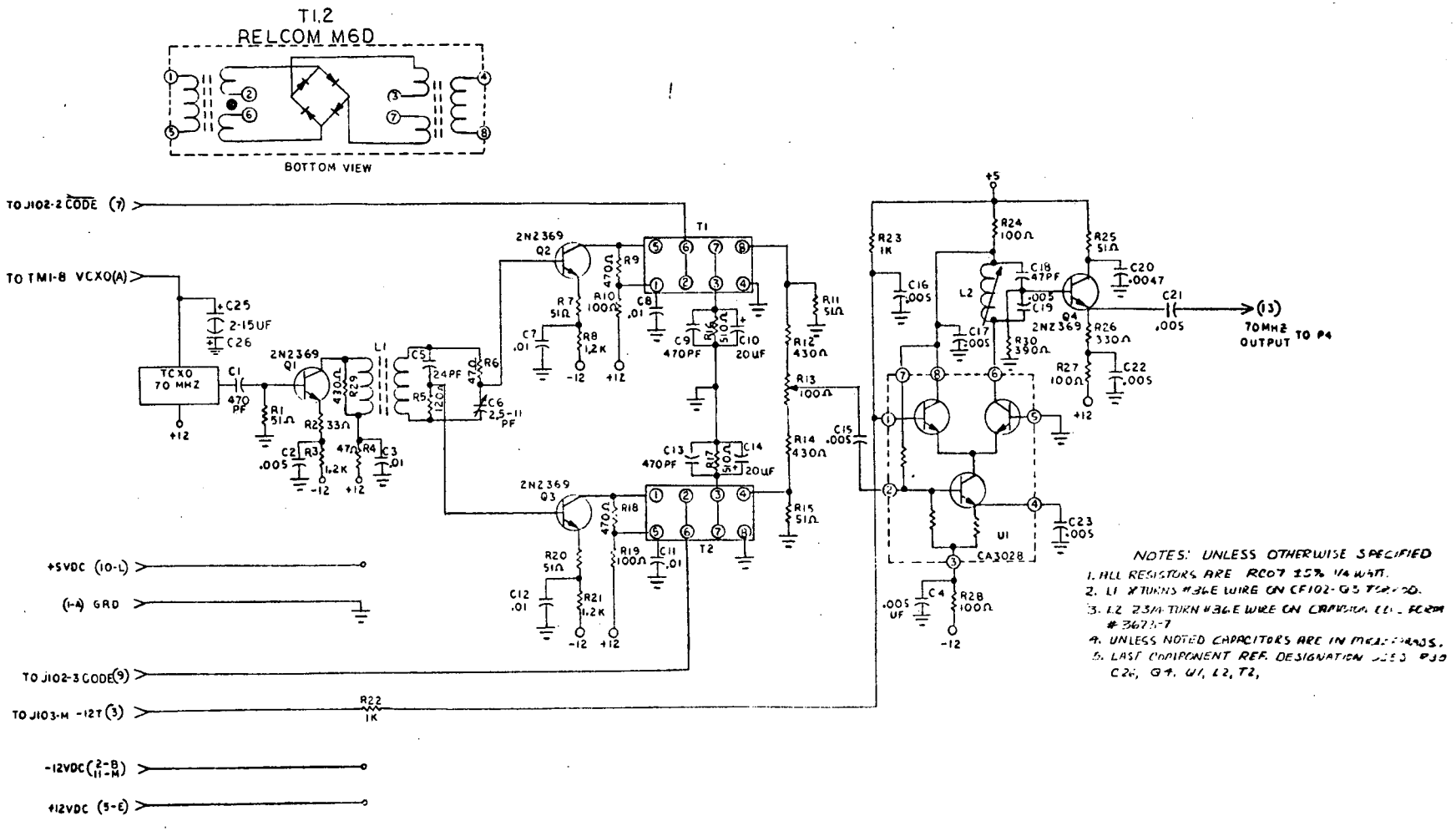


Figure 4-5. MX-290 Transmitter Multi-Mod Schematic Diagram

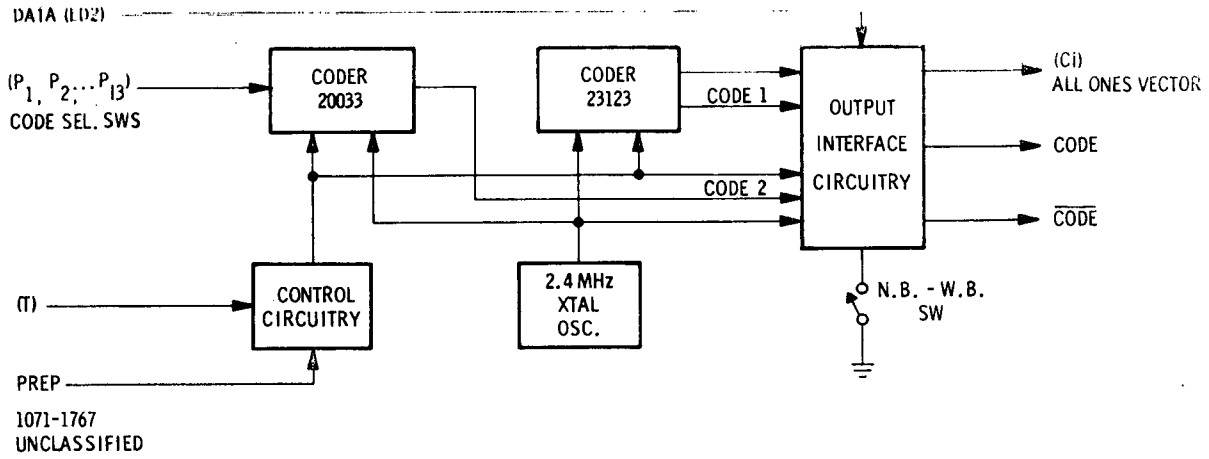


Figure 4-6. Block Diagram of MX-290 Coder Board (J102)

e. Inject the selected Gold code upon the reception of the (T) signal or when the PREP button is pushed and (T) is true.

Input/Output Routing

Figure 4-6 shows that J102 has four inputs and three outputs. The input ED2 is the selected data signal from the PDM board (J104). ED2 enters J102 at pin 10 and L goes to the interface network. The code select switch inputs (P_1, P_2, P_3, ... P_{13}) originate at the code select switches on the front panel and enter J102 at pins J, 9, K, 11, M, 12, N, 13, F, 7, H, 8 and P. Input (T) comes from the controller board (J103) and enters J102 at pin (6). Output signal (C_i) leaves J102 via pin (15) and goes to J103.

Input prep signal comes from the front panel PREP push button and enters the coder through pin (5).

Outputs code and $\overline{\text{code}}$ leave J102 via pins (3) and (2) and they go to multimod board J101. One board mounted control switch marked NB-WB is used to inhibit the PN sequence which will set the transmitter into a DPSK mode of operation. This is referred to as narrowband (NB) operation.

Description of Circuit Operation

As seen in figure 4-6, J102 contains two coders, a 2.4573 MHz crystal oscillators, control circuitry, and output interface circuitry. The 2.4573 MHz oscillator is used as the internal coder clock. It is also divided by two to form the output code clock. Each coder is a 13 stage maximal linear sequence generator. The coder feed taps have been selected so that the cross correlation properties of the family of codes generated are optimum. Coder 20033 is initialized by the settings of the code select switches via P1 through P13 and a given command from the control circuitry of figure 4-7 as

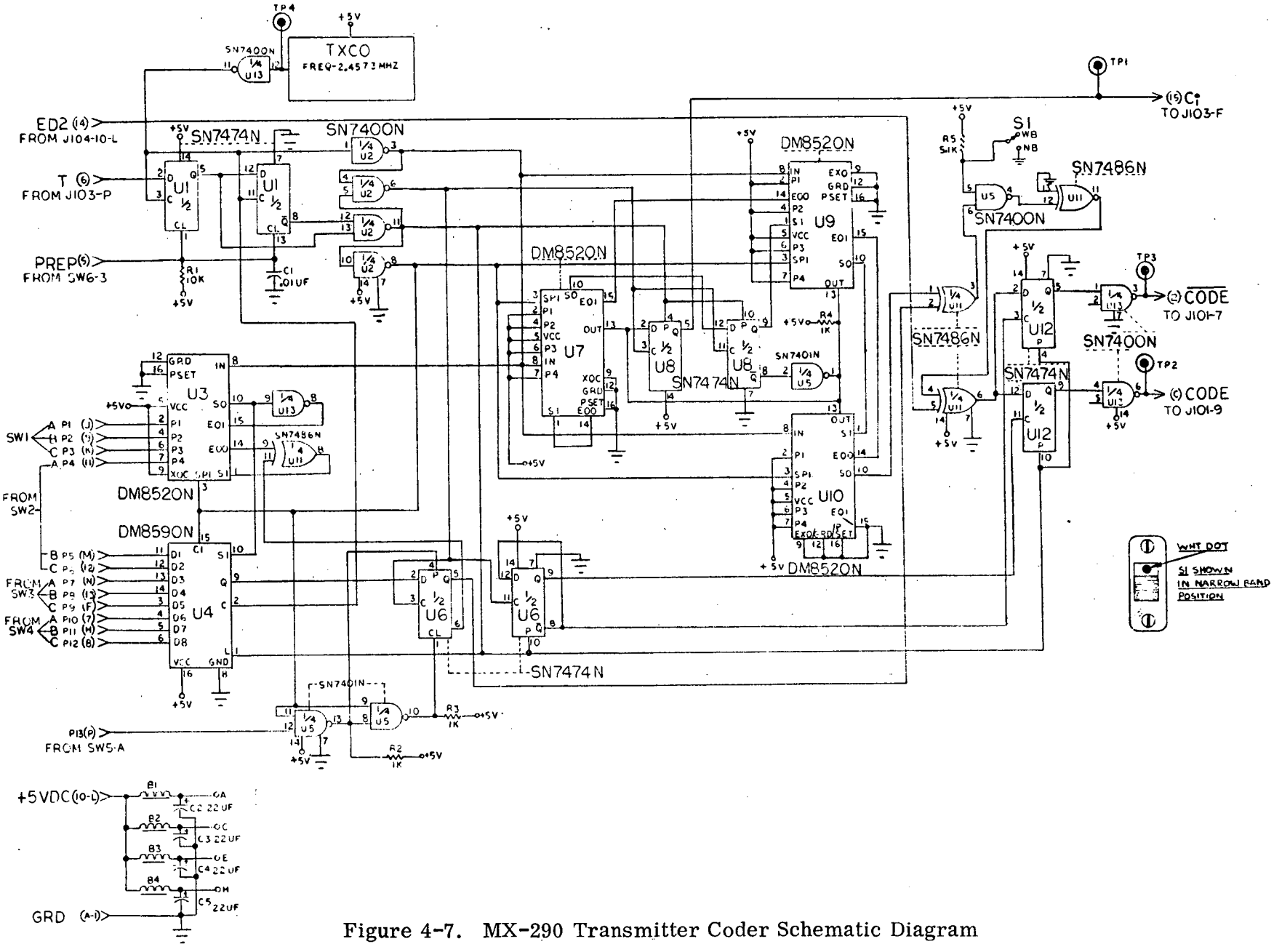
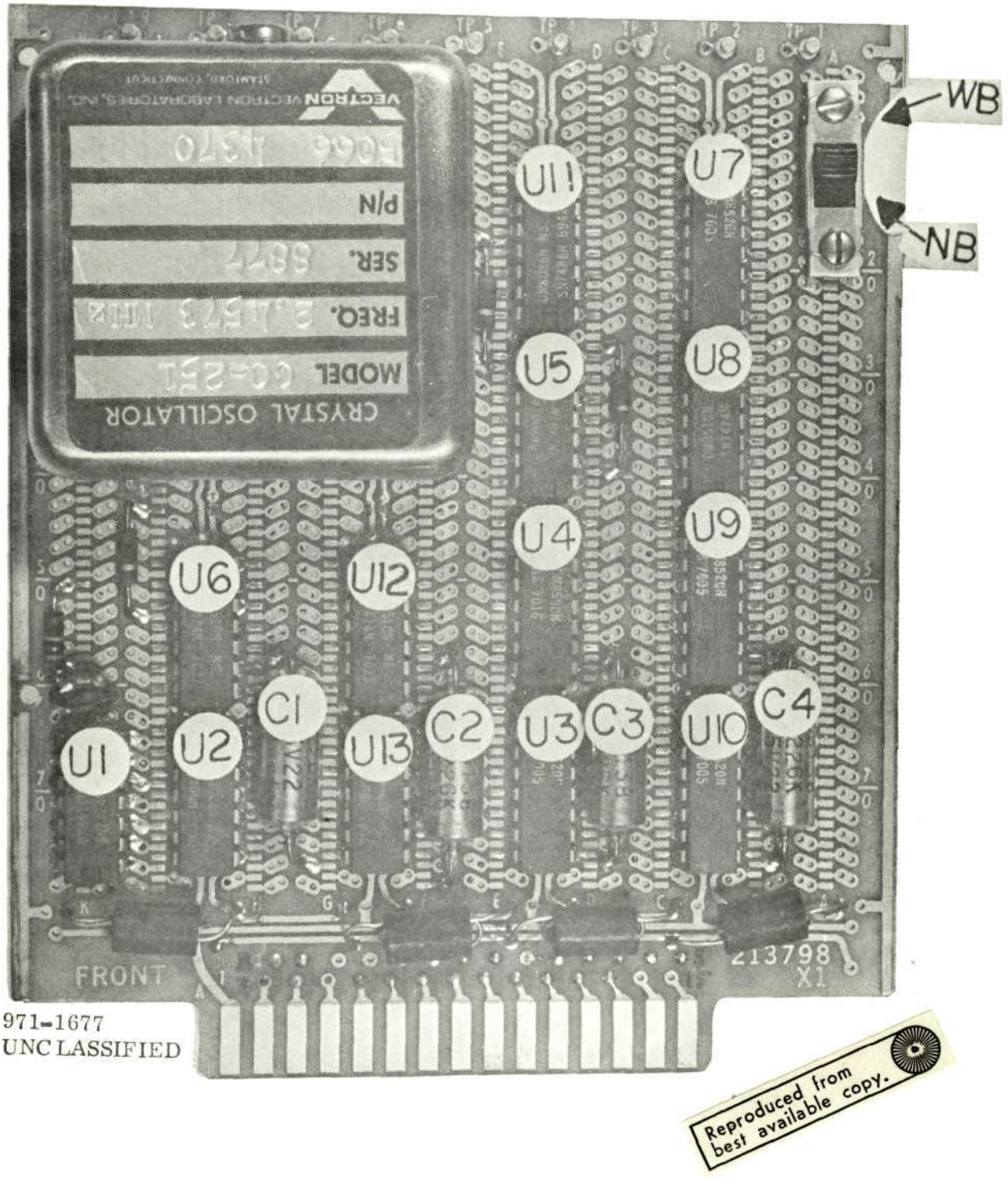


Figure 4-7. MX-290 Transmitter Coder Schematic Diagram



971-1677
UNCLASSIFIED

Figure 4-8. Transmitter Coder Board

listed in table 4-2. This command from the control circuitry also starts the other coder 23123 which is initialized in the "all ones" state. Hence, the two coders run with a given distance between them say, for example, their "all ones" vector as defined by the settings on the code select switches. The "all ones" vector (C_i) is decoded from coder 23123 and transferred to the interface circuitry which reclocks the C_i signal before it is transferred out via pin 15.

The coder (code, $\overline{\text{code}}$) outputs (figure 4-6) go to the output interface circuitry where they are first mod-two added to form a Gold code. This Gold code is then mod-two added with the data input ED2. The resulting signal is then transferred out to two output lines at a 1.229 MHz bit rate by two D flip-flops that are quadrature clocked. The signal out of each D flip-flop is therefore a double bit length signal consisting of alternate bits from the composite Gold code and data signals which are quadrature clocked. The 2 MHz oscillator signal in the output interface block is divided by two and to form the two quadrature clocks required above.

The control circuitry of figure 4-6 takes the (T) signal or the PREP signal and generates a sequence for initial conditioning the coder board. Each time the PREP button is pushed or a transistion occurs between transmit and stand-by a synchronous pulse of one bit length is formed by two D flip-flops. This signal is used to: (1) set the 23123 coder to its "all one" state, (2) crossinject the number on P1 through P13 into coder 20033, and (3) preset all the remaining flip-flops of the coder board. Also, when this initial condition pulse occurs the clock line is inhibited. The logic equations are written in reference to the element-pin call-out. For example, in figure 4-7, the output of U2 pin 6 is equal to the logic NAND of its inputs, U2 pin 12 and U2 pins 13, or as a logic equation $U2\text{-}8 = \overline{(U2 - 12) \cdot (U2 - 13)}$.

The circuitry of figure 4-6 which generates the initial conditions (IC) signal is accomplished by U1 and U2 on figure 4-6. The IC signal occurs at U2 pin 8 (U2-8). Hence IC = (U1-8) • (U1-5) or IC occurs when U1-5 and U1-8 are true. Assume that PREP is logic true (PREP button not pressed) then U1-5 is false and U1-8 is true if T is false. When T goes true then on the following (first) clock pulse U1-5 goes true - hence, IC goes true. On the next (second) clock pulse U1-8 goes false - hence IC goes false. When T goes false then U1-5 goes false, then U1-8 goes true, therefore no IC is generated. If the PREP button is pressed U1-1 and U1-13 go false and this forces

Table 4-2.

Figure 4-6 FUNCTIONAL BLOCKS	Figure 4-7 ACTIVE CIRCUIT ELEMENT
Control Circuitry	U1, U2
20033 Coder	U3, U4, U6-5, U5-13, U5-10, U13-8, U11-8
23123 Coder	U7, U8, U9, U10, U5-1
Output Interface Circuitry	U11-3, U11-6, U11-11, U5-4, U12, U13-6, U13-3, S1

U1-5 false and U1-8 true. Hence no IC. When the PREP button is released and T is true then we will follow the sequence that occurs when T goes true (same initial state as $\overline{T}$). When IC is true (U2-8 = 1) then U2-11 is false (U2-11 = 0). If U2-11 = 0 then U2-5 = 0 which inhibits the coder clock.

The 20033 coder is formed by U3, U4, U13-8, U11-8, U5-13, U5-10 and U6-5. What is inferred here is that all of U5 and U4 is used to form the 20033 coder with those logic functions associated with the following IC outputs U13-8, U11-8, U5-13, U5-10 and U6-5. U3 is a four bit Modulo-N-Divider and U4 is a parallel-in/series-out 8-bit register. Coder 20033 characteristic equation is $X^{13} + X^4 + X^3 + X + 1$ which requires serial modulo-two addition of stages 13, 4, 3, 1, 0. The first four stages and the serial mod-two addition is accomplished by U3, U13-8 and U11-8. U4 give the delay for 8 bits and U6, U5-8, and U5-13 form the last stage. The 20033 coder output is U6-5.

Coder 23123 is generated by U7, U8, U9, U10 and U5-1. U10-10 is the output of 23123 coder which goes to U11-1. U11-3 is the modulo-two addition of the two PN codes (Gold code). U5-4 and U11-11 form the Gold code inhibit gate with the NB-WB switch. U11-6 is the composite signal which is the modulo-two addition of the data and Gold code. U6-9 divides the coder clock by two. U12-5, and U12-9 are the D flip-flops that accept alternate bits from the composite signal to form the quadrature clocked output codes.

4.1.1.8 MX-290 Controller Board (J103)

Board J103 is a universal printed circuit board with jumper connections. In the following description figures 4-9, 4-10, and 4-11 are used to describe this unit.

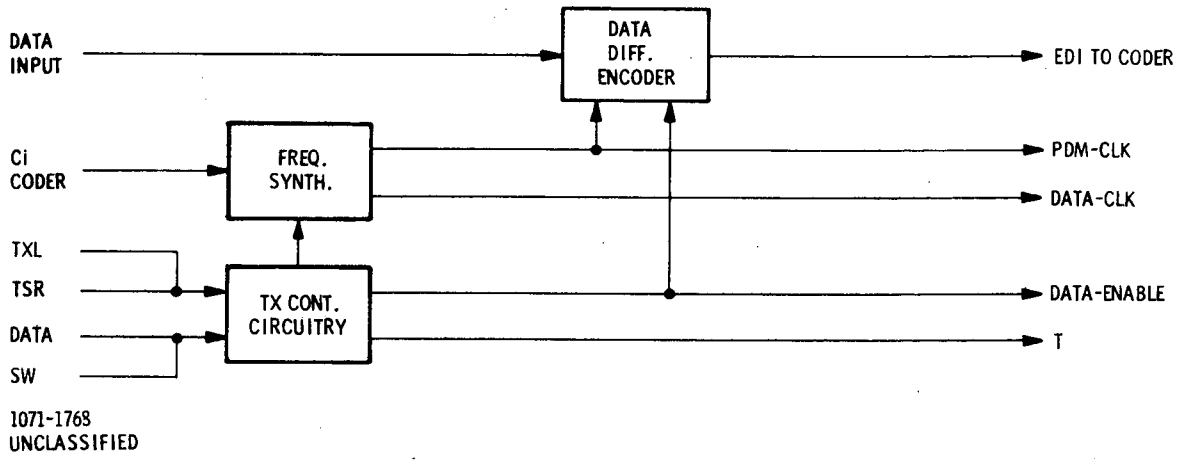


Figure 4-9. MX-290 Controller (J103) Block Diagram

Purpose of J103

The purpose of J103 is to:

a. Convert the digital data input to TTL levels and differentially encode the data. Also inhibit the encoded data for eight seconds after the (T) command has been initiated.

b. Generate the digital data and PDM clocks. Also, transfer out the selected data clock via MIL-STD-188B.

c. Generate the transmit command signals.

Input/Output Routing

Figure 4-10 and figure 4-9 show that J103 has six inputs and five outputs. The data input J103-2 comes from the barrier strip on the back, or the BNC connector on the front. This is the digital data input line. Input 24DR and 12DR, J103-3 and J103-5, are the 2400 data rate command and the 1200 data rate command which come from the front panel DATA RATE switch. The (C_i) input J103-6 is the "all ones" vector from the coder J-102. TXL input, J103-14, is the local transmit command which is derived from the front panel TX/STD-BY switch or the MIC jack via a push to talk button. The data clock output, J103-4, goes to the front panel DATA OUT BNC and to the rear panel barrier strip. Output ED1, J103-7 is the differentially encoded digital data that goes to the PDM board. The 9.6 kHz PDM clock, J103-4, is the PDM clock and it goes to the PDM board. The (T) signal, J103-P, is the logic level transmit command signal and it goes to the coder J102. Output -12T, J103-11, is the -12 volt transmit command which goes to the multi-mod J101.

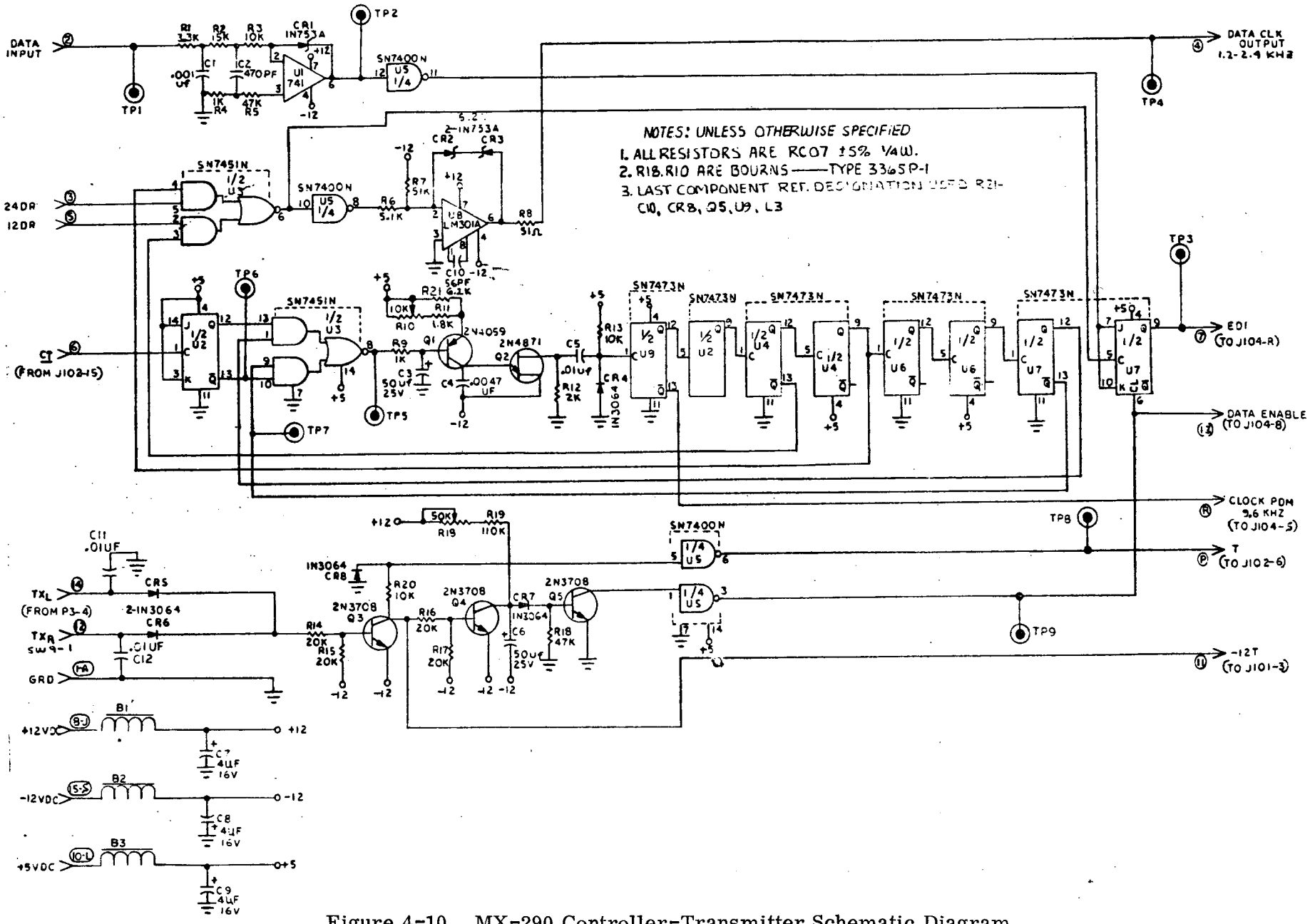


Figure 4-10. MX-290 Controller-Transmitter Schematic Diagram

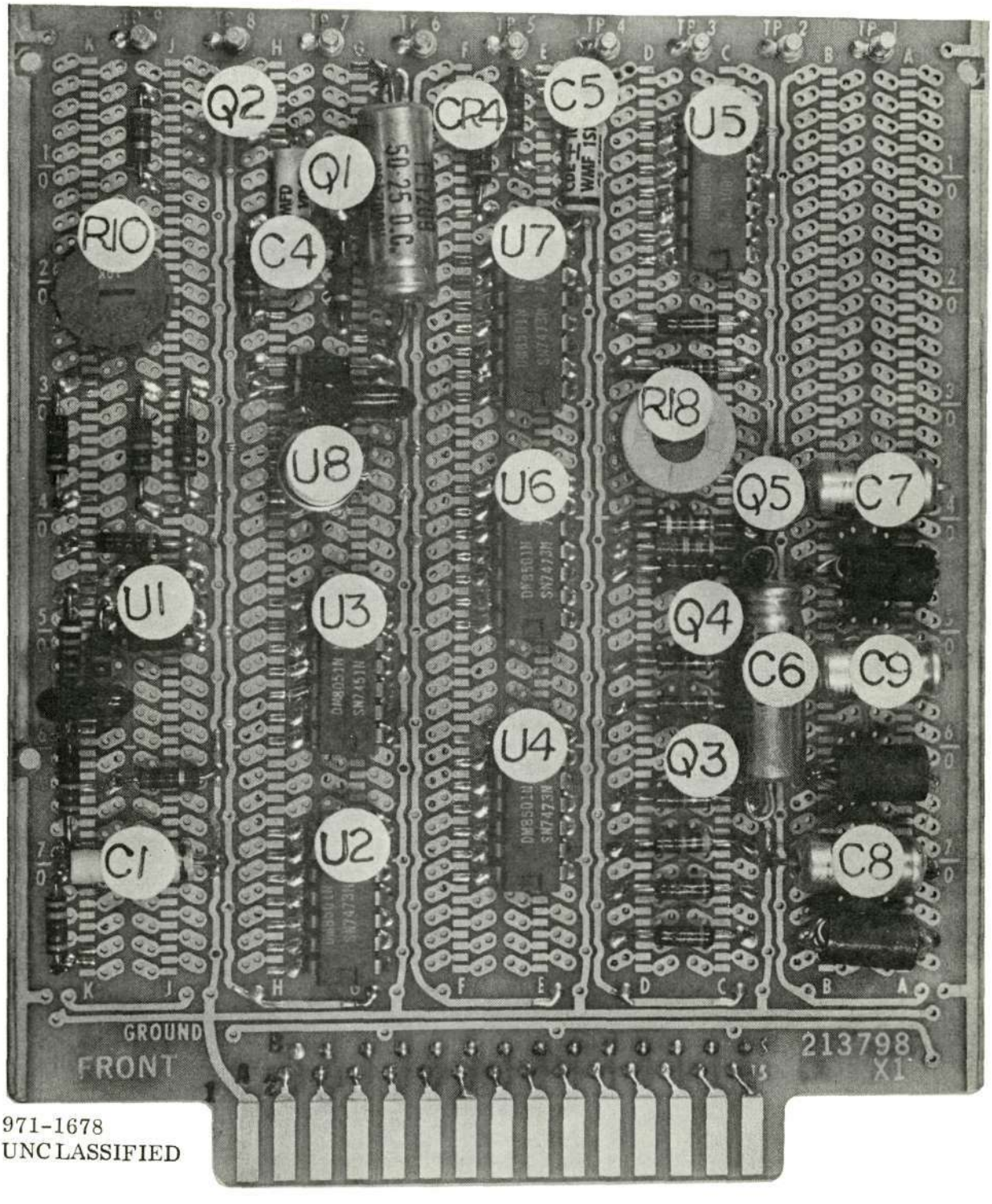


Figure 4-11. J103 Transmitter Controller

The data enable, J103-12, output command occurs eight seconds after (T), the transmit command. This signal is used to inhibit the transmission of data for eight seconds after the initiation of transmit. This signal goes to the PDM board.

Description

The digital data input is filtered and converted from MIL-STD-188B to TTL logic level by U1 which is a type 741 operational amplifier. This amplifier has a low pass filter input network and a 4.3 volt zener as its feedback elements. Such a configuration will cause the output of U1, i.e., U1-6 to be zero volt for all positive going signals at J103-2. Also, as J103-2 goes negative the operational amplifier will multiply the input signal by its open loop gain until the output reaches zener diode breakdown voltage. The output will then be clamped to this value. U3-11 is a NAND gate that couples the converted data input to pins U7-7 and U7-10 which is the J&K inputs to a JK flip-flop.

The differentially encoded data appears at terminal U7-9. Differential encoding implies here the following:

- When logic "one" appears at the input - change either the sign or logic state of the output.
- When logic "zero" appears at the input - maintain either the previous sign or logic state of the output.

Either 24DR or 12DR input signals is true —hence, this will allow the 2400 Hz or 1200 Hz clock at U3-6 (a modulo-two addition). This signal, U3-6, is then used to clock that digital data encoding flip-flop U7-9. U3-6 is also transferred to MIL-STD-188B via U8. U8 is a 741 OPA with a resistive input and back-to-back zeners for the feedback network. The zeners will bound the output signal level to that zener voltage plus a diode drop (the other zener is forward biased). The slew rate, rise and fall time, were controlled by selection of the compensation caps. To generate the data clocks from the all ones vector via multiplication the phase lock loop procedure was used. The C_i pulse is divided by two then modulo-two added to a 19.2 kHz VCO counted down to 150 Hz. This mod-two output is filter by the loop filter and used as the control voltage for the 19.2 kHz VCO. U2-12 is toggled, by the C_i pulse to form the 150 Hz square wave. U3-8 (a mod-two adder) is the loop multiplier and R9 and C3 form the loop filter with Q2 a unijunction VCO as the loop VCO. U9-12, U2-9, U4, U6 and U7 form the binary countdown circuits required.

Consider how the various transmit command signals are shown on figure 4-10. When TX_L or TX_R is grounded, Q3 will saturate and U5-6 goes to a logic one level, the T command. Also Q4, who was saturated, is shut-off which causes C6 to charge towards the +5 volt supply. When C6 exceeds +1.4 volts, Q5 saturates causing U5-3 to go to a logic one level. It takes eight seconds for C6 to charge from -12 volts to +1.4 volts. U5-3 is the data enable signal used to inhibit data out for eight seconds after the T command is received. Data enable is also sent out to the PDM board.

4.1.1.9 PDM Conditioner (J104)

In the following description, figures 4-12 and 4-13 are used to describe this unit.

Purpose of J104

The purpose of J104 is to:

a. Convert the mike (audio) input signal to suppressed clock pulse duration modulation (SCPDM). Also pre-emphasis, AGC and speech conditioning prior to modulation.

c. Generate ED2.

Input/Output Routing

There are seven inputs and one output to J104. The mike input, J104-2, B, comes from the front panel. The 9.6 kHz input (J104-15, S) comes from the controller, which is the PDM clock. The PDM switch (J104-12, N) and DATA switch (J104-13, P) come from the front panel switches. Input ED1 (J104-14, R) and data enable (J104-8, J) come from the controller board. ED2 is the only output and it is the selected encoded data signal that goes to the coder J102. The selected encoded data signal is either SCPDM or differentially encoded digital data.

Description

From figure 4-13, the mike input signal (J104-2, B) is terminated by 150 ohm resistor R1, and then buffer-amplified by U1 a 741 OPA. U1 has an in-band gain of 21 times whose output goes to OPA U2. The output of U2 is transformer coupled to a thick film AGC/speech conditioner network U3. The output of U3 (U3-30) goes to U4 which is also a thick film circuit. U4 is a 2500 Hz active low pass filter which has unity gain.

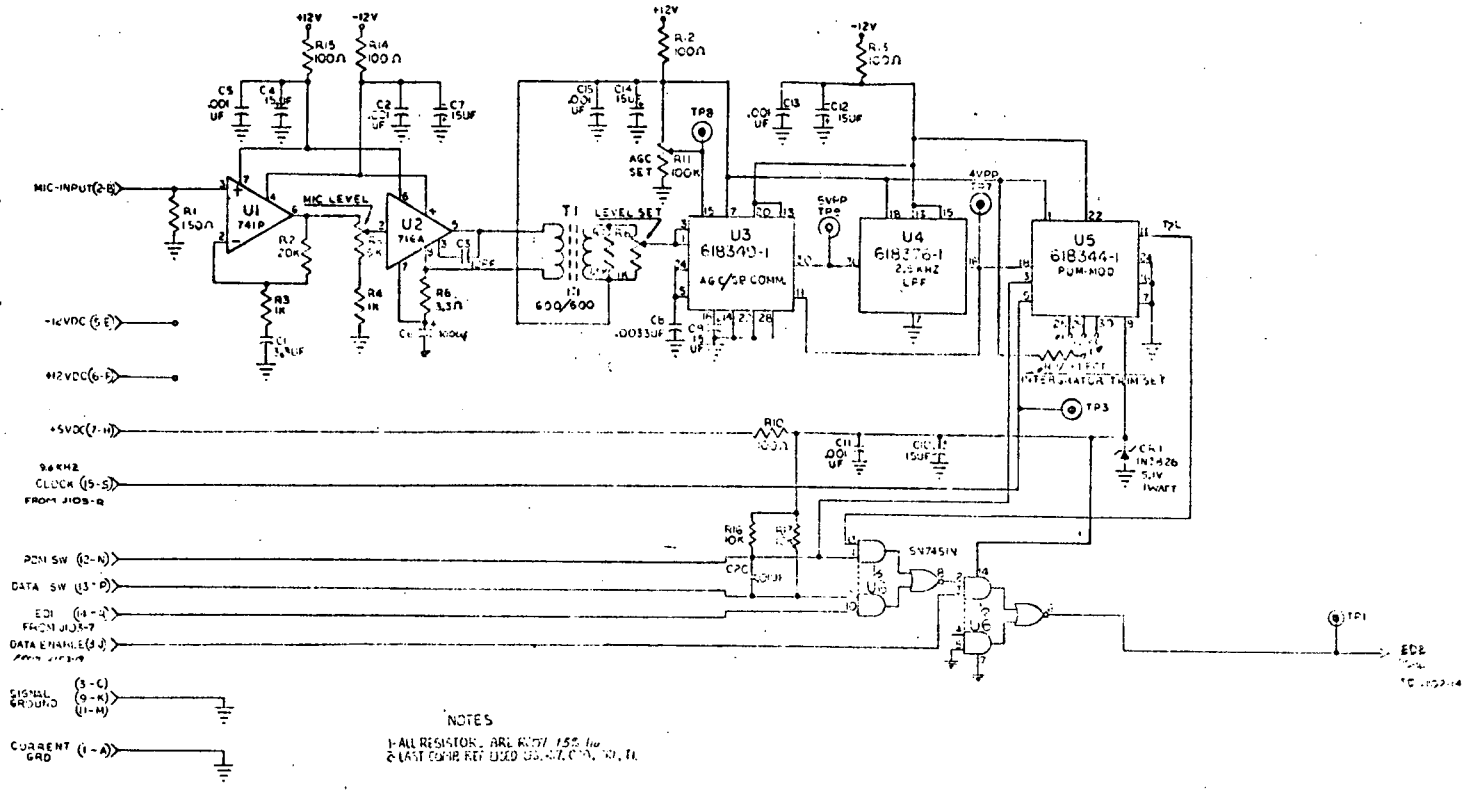
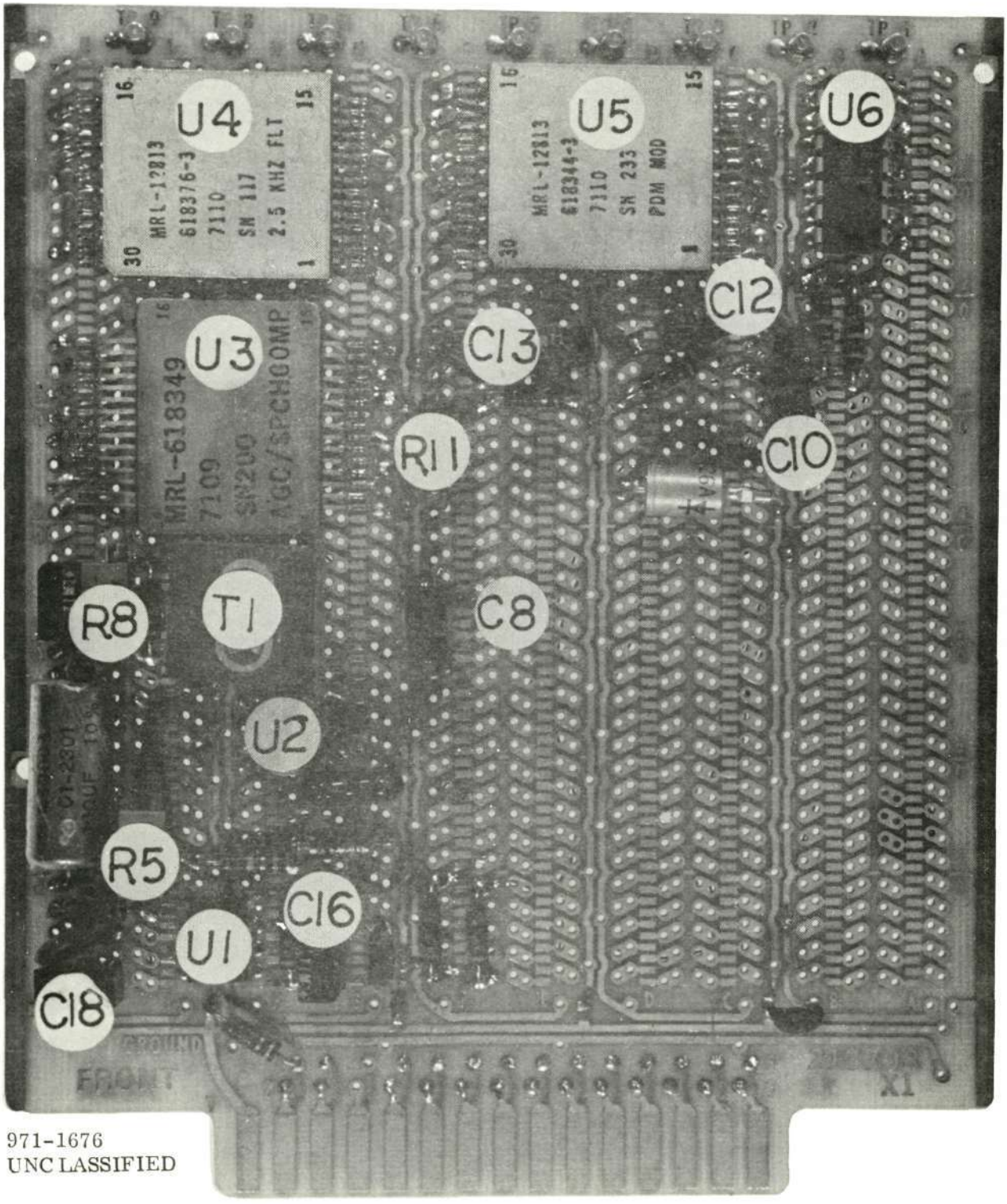


Figure 4-12. MX-290 TX PDM Conditioner Schematic Diagram



971-1676
UNCLASSIFIED

Figure 4-13. J104 Transmitter PDM Board

The output of U4 is fedback to U3 as the signal to AGC, and to U5, a thick film circuit. U5 is the SCPDM modulator. The processed audio signal at the input to U5 is first converted to PDM and then the clock is removed. The clock is removed by modulo-two addition of the PDM signal with the squarewave clock signal.

U5 output (U5-11) goes to U6. U6, a mod-two adder, forms ED2, the selected encode data going to the coder. The encoded data signals available for selection are ED1, the differentially encoded digital data, and the SCPDM signal. The PDM switch/DATA switch signal is used as the select signal.

4.1.2 CHASSIS PHYSICAL LAYOUT

The transmitter subunits are housed in a cabinet having dimensions 9 x 7 x 13 inches. The physical location of the boards and the power supplies are shown in the top inside view of figure 4-14. The internal adjustments are also indicated in this figure.

4.1.3 SIGNAL LOCATION CHARTS

For the purpose of maintaining and servicing the transmitter unit a number of test points are provided on the top and at the card connectors on the bottom of the card cage. From the top, the signals can be monitored at test points located at the top of each plug-in board. A call-out of each test point is given in figure 4-15. The definition of symbols used to identify the signal at each test point is presented in Appendix A.

Also, a number of useful test points are available on the card connectors. These test points can be easily accessed from the bottom of the card cage. The diagram showing locations of the various signals in terms of their symbols is given in figure 4-16. Also, signal wire routing on a point-to-point basis is shown in figure 4-17. The explanation of these symbols is also given in Appendix A.

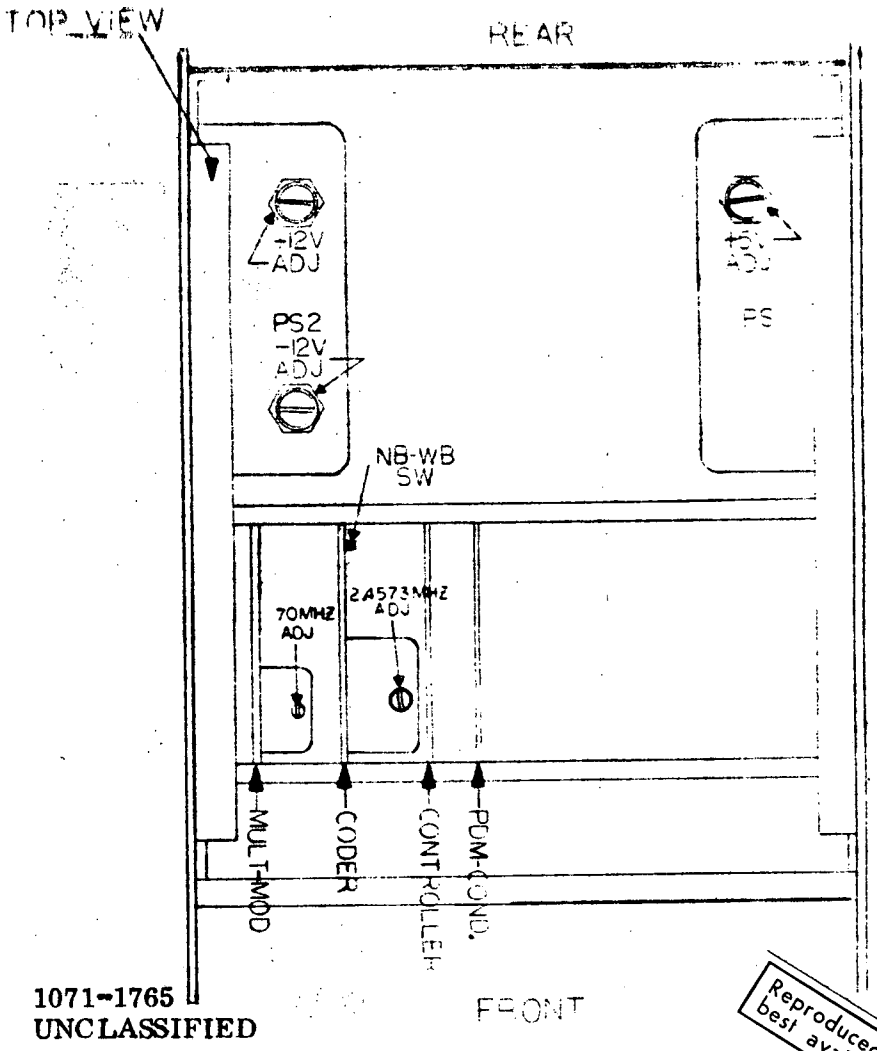


Figure 4-14. Chassis Physical Layout

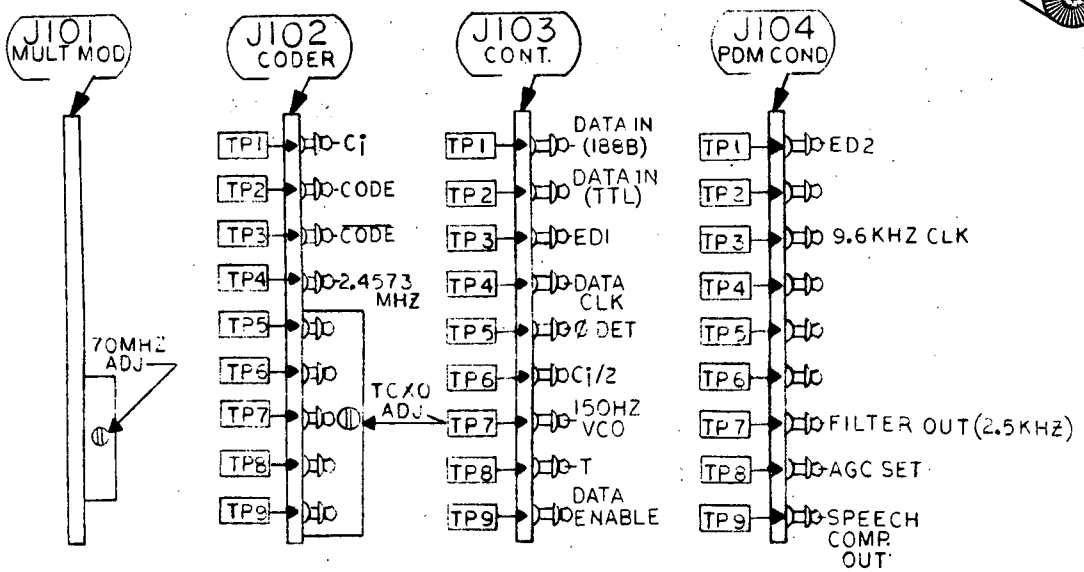


Figure 4-15. MX-290 Transmitter Test Points and Adjustments

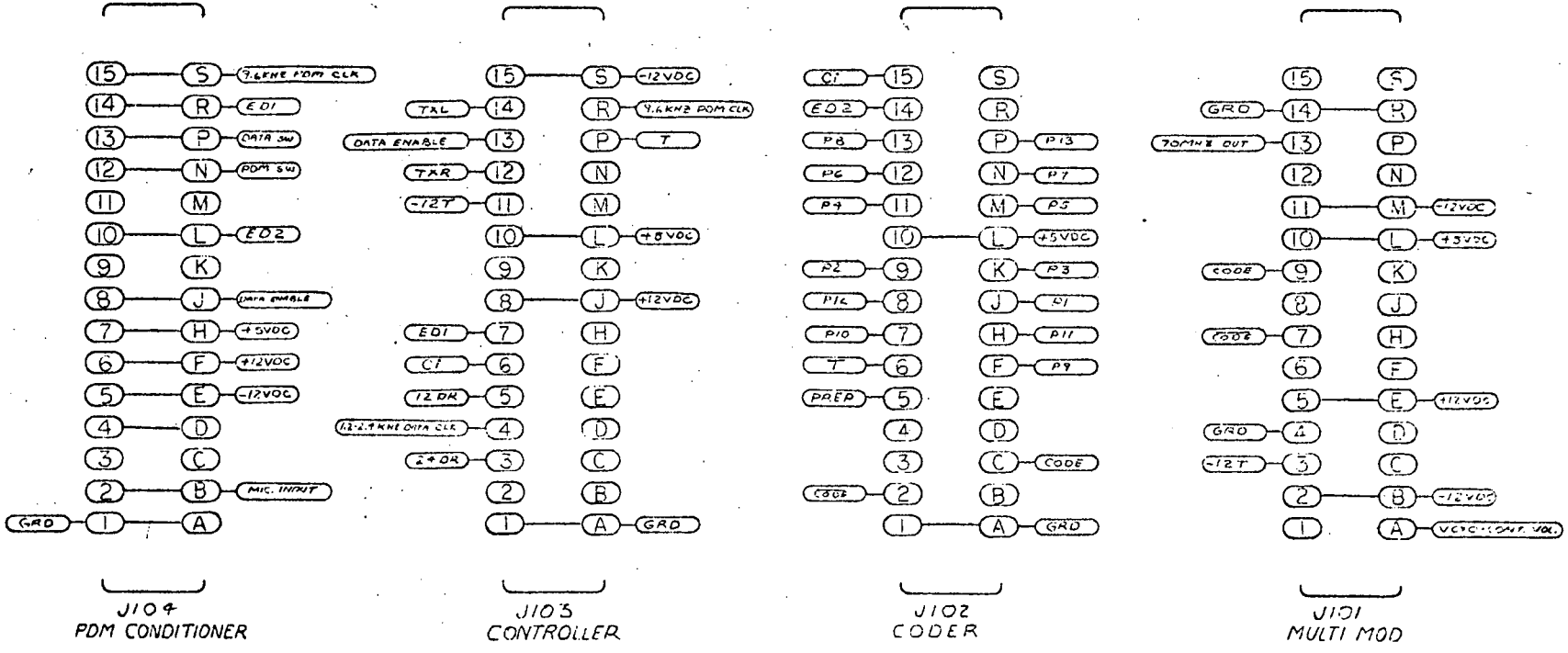


Figure 4-16. MX-290 Function Symbol Location Diagram

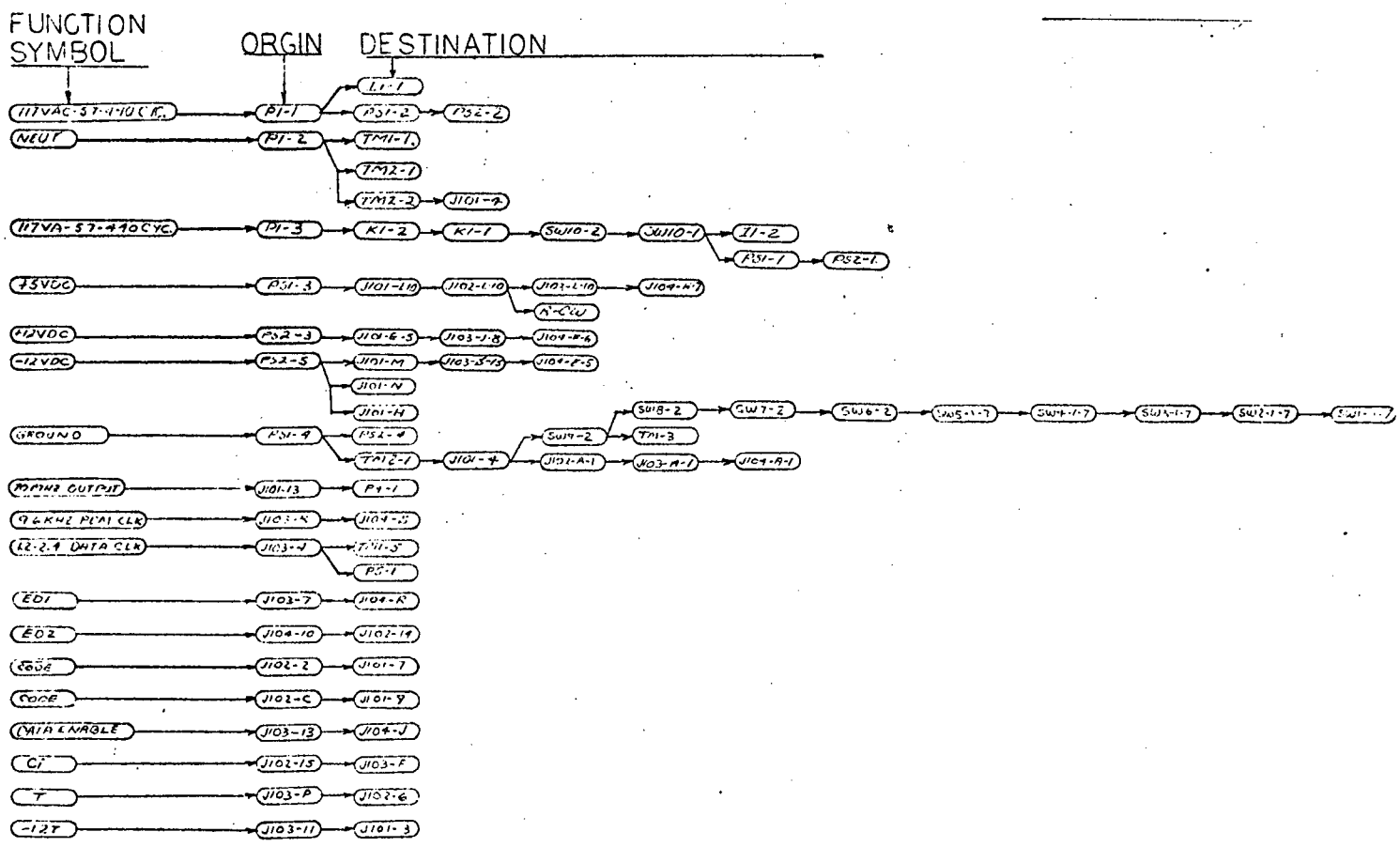


Figure 4-17. MX-290 Function Symbol Routing Diagram

4.2 MX-291 RECEIVER DESCRIPTION

4.2.1 INTRODUCTION

The receiver consists of seven plug-in cards and one 70 MHz IF amplifier can. The description of these subunits follows. For this description, refer to figure 4-18. As seen in the block diagram, the receiver consists of eight subunits, two power supplies, a front control panel, and a rear access panel. In addition to these subunits, which are located in the chassis with its interconnecting cables and wires, an external amplifier speaker unit is provided. The speaker plugs into the AUDIO OUT jack.

The eight functional subunits of the receiver are:

a. IF amplifier
b. Controller board
c. Data processor board
d. Coder board
e. Digital receiver
f. Clock board
g. Multi-mod board
h. PDM processor board

Some of these boards are practically identical to their counterparts in the transmitter unit such as the coder and multi-mode boards. The function of these boards are briefly described below. For the description, refer to figure 4-18.

4.2.1.1 70 MHz IF Amp.

The 70 MHz IF amp performs the following functions:

a. Amplifies and filters the 70 MHz input signal.
b. Correlates the 70 MHz input with a 72 MHz reference and translates it to a 2 MHz second IF.
c. Amplifies and filters the 2 MHz signals.

4.2.1.2 Controller

Controller board performs the following functions:

a. Generates the AGC signal for the IF board.
b. Generates the sync signal.
c. Generates the noise meter signal.

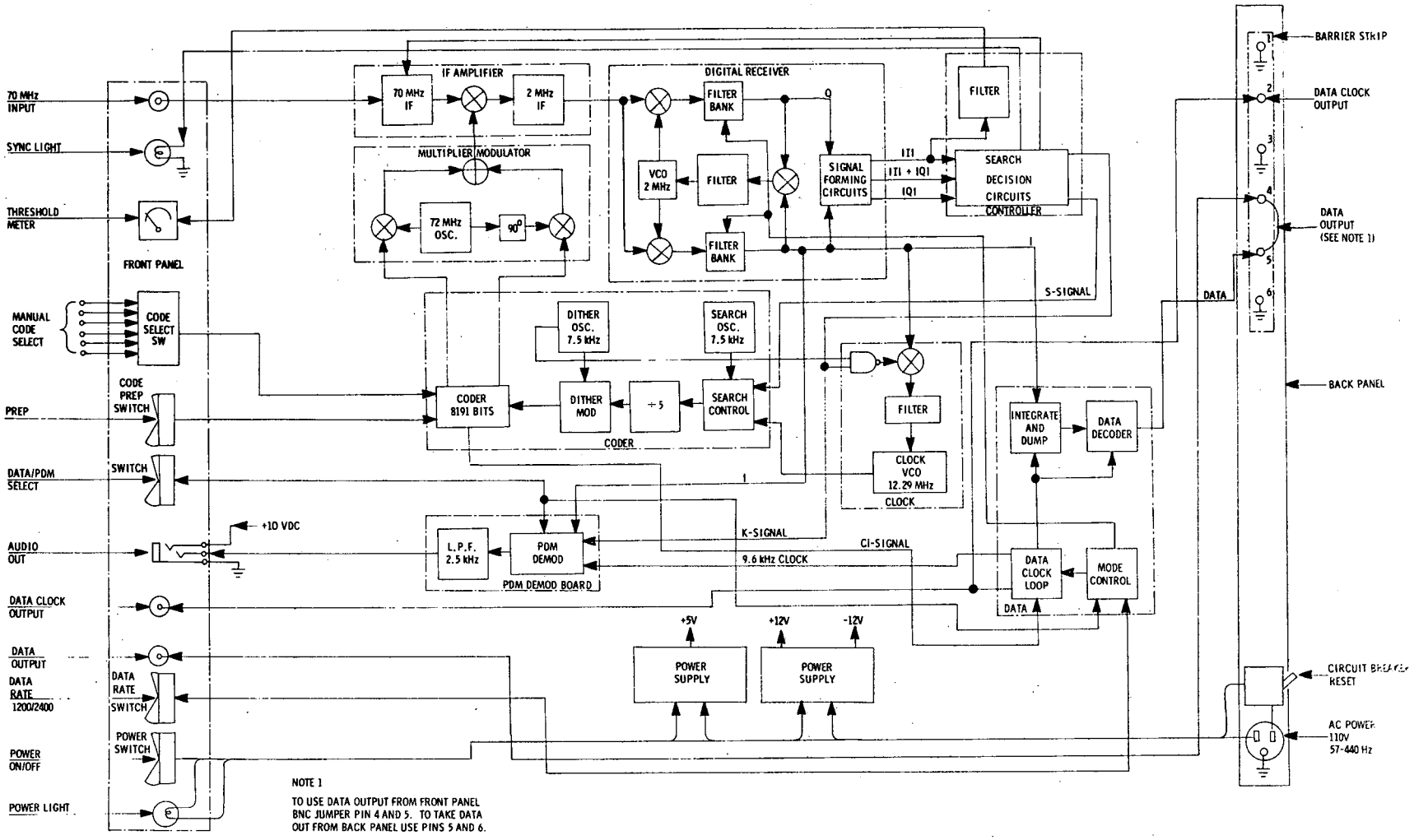


Figure 4-18. MX-291 Receiver Block Diagram

4.2.1.3 Data

The function of the data board is to generate the 1200 or 2400 data clock signal from the coder's "all ones" vector and buffer out. This is accomplished by a phase lock loop whose VCO runs at 4800 Hz. The extraction of the 9400 Hz clock needed for the PDM data demodulator is also performed by the data board. The mode control subunit located on this board performs the function of sending commands to the digital receiver board for selection of proper filter time constrants. The data itself is extracted from the incoming data stream by means of an integrate and dump circuit which is followed by a differential decoder network.

4.2.1.4 Coder Board

Similar to its transmitter counterpart, the receiver coder board performs the following:

a. Generates codes preselected at the front panelcode selector switches.

b. Forms two quadrature clocked versions at the selected code, each of these versions displaced with respect to each other by one-half the run length.

Furthermore, to provide the receiver clock tracking, several subunits are are added to this board. The function of these subunits are:

a. To advance the coder clock with respect to the clock of the received code for the purposes of implementing the initial search procedure.

b. To provide the so called "dither" which consists of back and forward displacement of the reference code with respect to received code. This function is performed for the clock tracking after initial acquisition.

4.2.1.5 Digital Reciever

The digital receiver card consists of a Costas loop, and envelope detector $|I| + |Q|$, and the inphase $|I|$ and quadrature $|Q|$ detectors. The Costas loop is reconstructed from the signal's sideband phase of the received suppressed carrier, tracks this phase utilizing the "Q" signal, and recovers coherently the envelope of the received signal, thus, providing the "I" signal. In essence, the Costas loop performs a linear translation of the 2 MHz centered signal to IF frequency of zero cycles, i.e., translates the signal's sidebands back to the baseband.

4.2.1.6 Clock Board

The function of this board is, in addition to providing the 12.29 MHz signal, which is counted down to the proper code clock frequency, to demodulate the "dither" signal which is used for keeping the incoming and locally generated reference in synchronism. This dither signal is extracted from the I channel output supplied by the digital receiver board.

4.2.1.7 Multi-Mod Board

This board is identical to its counterpart in the transmitter with the exception of the center frequency which is 72 MHz. The oscillator which provides this 72 MHz signal is fixed tuned.

4.2.1.8 PDM Processor Board

This board accepts the binary data stream which represents the encoded PDM voice and converts this data stream to an analog voice signal. All the necessary post demodulation filtering is also performed by this board. The analog voice signal is supplied to the audio jack on the front panel.

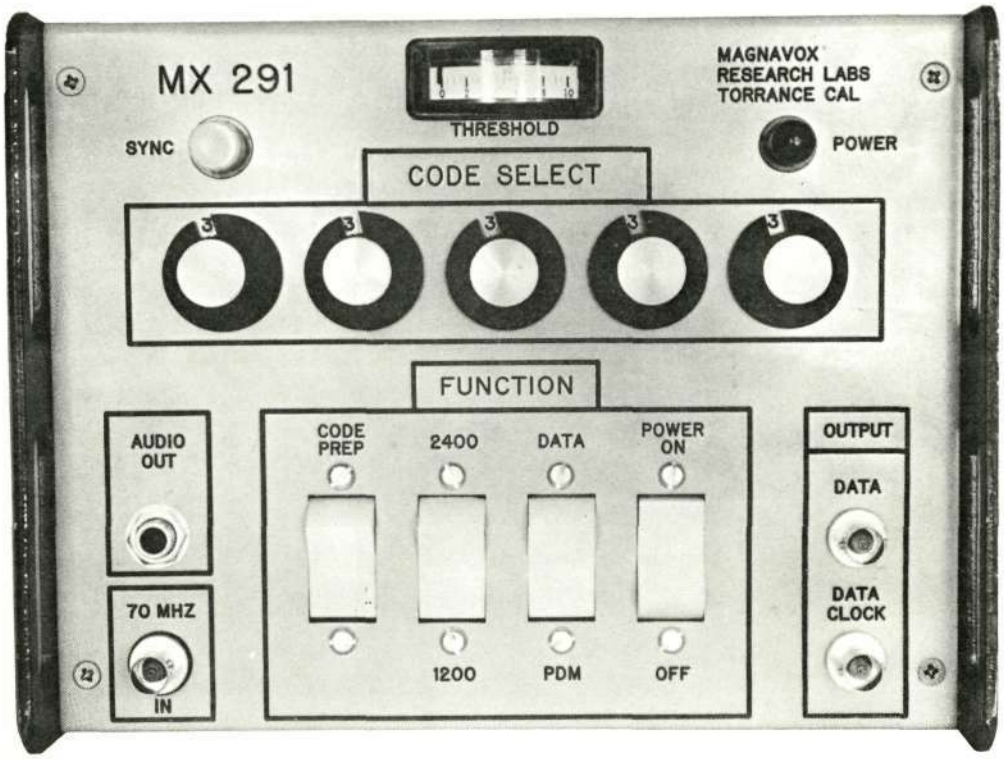
4.2.1.9 Front and Rear Panels

All of the receiver operator controls are located on the front panel of the chassis. As can be seen from figure 4-19, all of the controls are clearly labeled and are self explanatory. However, a brief description of each control and input / output jacks is given in table 4-3. For this discussion, a reference should be made to the figure showing the front panel and also to the figure showing the overall block diagram.

As shown in figure 4-20, the rear panel layout of the receiver unit is identical to the transmitter unit, with the exception of the BNC connector.

4.2.1.10 70 MHz Amplifier

The 70 MHz amplifier is assembled on a P.C. board. The P.C. board is inserted into a silver plated can with all power supply leads filtered by feedthrough capacitors. Al RF signals are routed through bulkhead mounted subminiature snap-on type connectors ("Conhex"). See figure 4-41 for location.



971-1668
UNCLASSIFIED

Figure 4-19. MX-291 Receiver Front Panel

Table 4-3. MX-291 Front Panel Control Descriptions

Item	Function
POWER ON/OFF switch and indicator	AC power on/off switch
DATA/PDM switch	Data or PDM voice output select switch
DATA RATE 2400/1200 switch	Digital data rate select switch
CODE PREP switch	This switch is used to initialize the code shift register states after initial power turn on.
CODE SELECT switches	The five CODE SELECT switches are used to program the coders to generate one of the available 8192 PN codes. The selected code is always identical to the one selected on the corresponding transmitter.
AUDIO OUT jack	Provides demodulated voice output to an external speaker

Table 4-3 (Continued)

Item	Function
70 MHz IN connector	Allows input of the 70 MHz signal.
OUTPUT DATA connector	Provides digital data output when in the digital data clock
DATA CLOCK connector	Output from the digital data clock.
SYNC indicator	Lights when the local code coincides with the phase of the incoming received code.
THRESHOLD meter	Indicates synchronism condition and strength of the received signal. The latter indication is obtained by measuring the content of the noise in the Q channel of the digital receiver.

Purpose

The 70 MHz amplifier performs the following sequence of operations:

a. Regulates and band restricts the 70 MHz input signal.

b. Correlates and translates the 80 MHz input with a 72 MHz reference, which translates to 2 MHz.

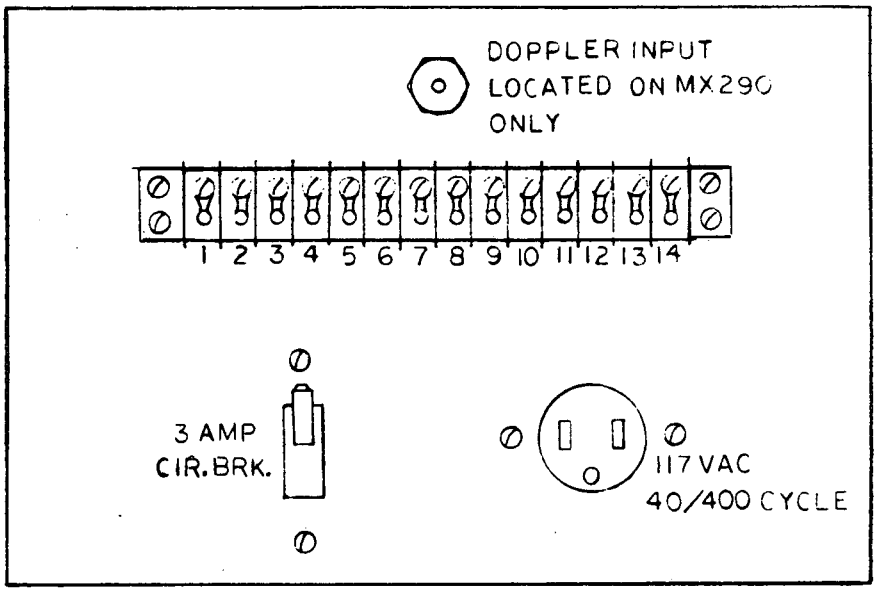
c. Amplifies and band restricts the 2 MHz signal.

Input/Output Routing

From figure 4-21, note that there are two RF and one control signal as inputs. The 70 MHz input comes from the front panel 70 MHz BNC input via subminiature coax. The 72 MHz RF input comes from J202 via subminiature coax. The AGC control voltage comes from J204. The signal output 2 MHz goes to J205 (digital recorder) via subminiature coax.

Description

Figure 4-22 is a general block diagram of the 70 MHz amplifier. Figure 4-21 shows that the 70 MHz amplifier consists of three tuned CA 3005 amplifier stages with AGC. A list follows that shows the overall system AGC range in terms of the 70 MHz input signal level and the output level, at the post correlator test point, (normalized).



CONNECTIONS ON BARRIER STRIP MX-290

*PIN 1. SAFTY GROUND

PIN 2. DATA IN BACK PANEL

PIN 3. SHIELD GROUND

PIN 4. DATA IN FRONT PANEL

JUMPER IF FEEDING DATA FROM FRONT PANEL BNC. REMOVE IF FEEDING DATA FROM REAR PANEL THRU PIN 2.

PIN 5. DATA CLOCK OUT

PIN 6. TXR, REMOTE TX.

PIN 7. R-S, DOPPLER CONTROL SWINGER

PIN 8. VCO CONTROL LINE

PIN 9. REMOTE DOPPLER INPUT BNC BACK PANEL

SEE NOTE

*PIN 1. LEFT SIDE WHEN FACING BACK PANEL

NOTE: WHEN USING DOPPLER CONTROL ON FRONT PANEL, JUMPER PIN 7 and 8.
IF REMOTE DOPPLER IS USED JUMPER PIN 8 and 9.

1071-1769
UNCLASSIFIED

Figure 4-20. Rear Panel Layout

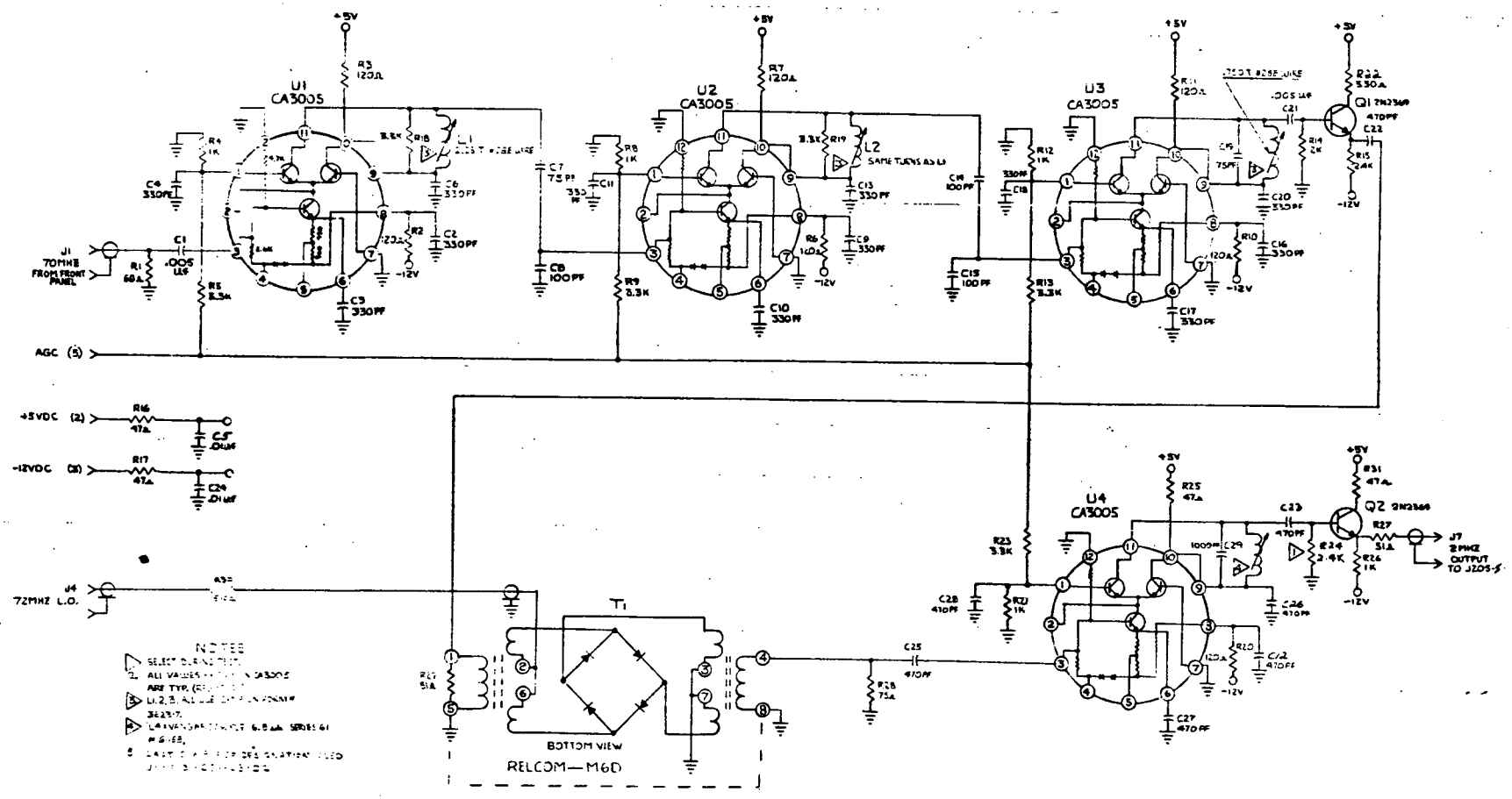


Figure 4-21. MX-291 Receiver, 70 MHz Amplifier Diagram Schematic

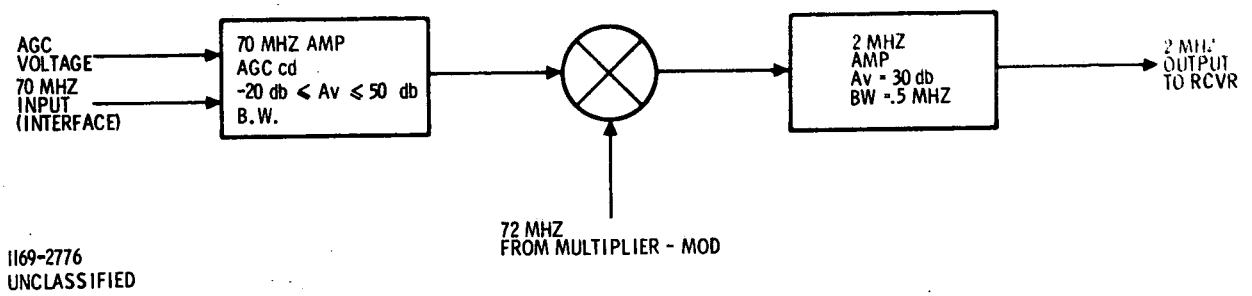


Figure 4-22. 70 MHz Amplifier Block Diagram

AGC Range

70 MHz Input Level	Normalized Post Correlator Output
- 20 dBm	+ 0.2 dB
- 70 dBm	0 dB
- 82 dBm	0 dB
- 83 dBm	- 1 dB
- 84 dBm	- 2 dB
- 85 dBm	- 3 dB

The 70 MHz amplifier has a minimum gain of 50 dB, with a 2.5 MHz 3 dB bandwidth. The correlator has a conversion loss of 7 dB, and the two megahertz amplifier stage has a gain of 30 dB. The signal out at 2 MHz is set for - 15 dBm (signal only) under operational conditions. With the above output constraints, this sets the minimum input to the system below - 80 dBm. The correlator is a Relcom 6D mixer. The two megahertz amplifier is a CA3005 tuned, 150 kHz 3 dB bandwidth amplifier, with a 2N2369 emitter follower buffered output.

4.2.1.11 Coder Board J201

The following discussion of J201 is related to figures 4-23, 4-24, and 4-25.

Purpose

The purpose of J201 is to:

a. Generate the selected Gold code.

b. Construct two quadrature clocked phases of the Gold code that are phased by a difference of one half the run length (8191/2).

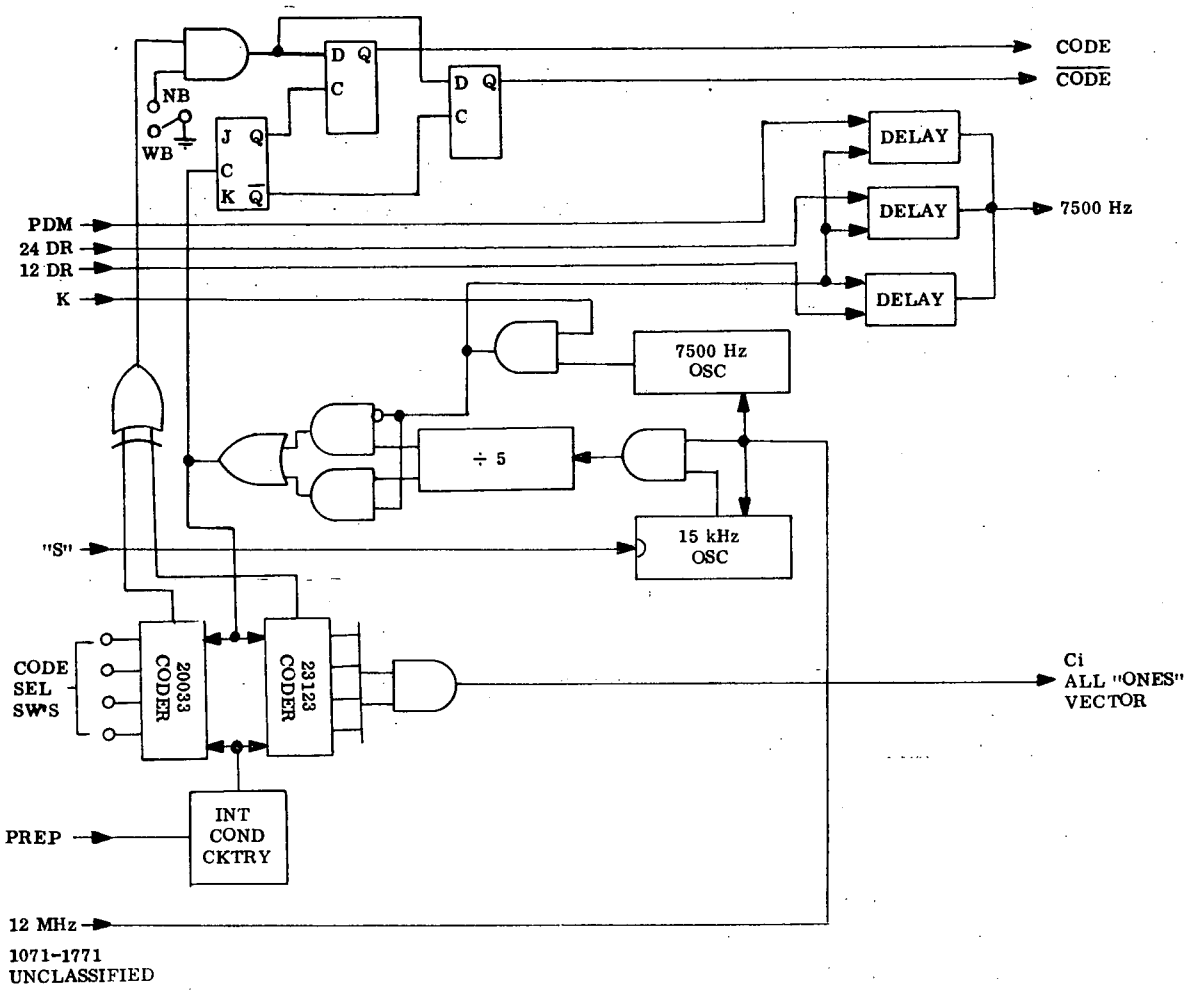


Figure 4-23. Receiver Coder J201

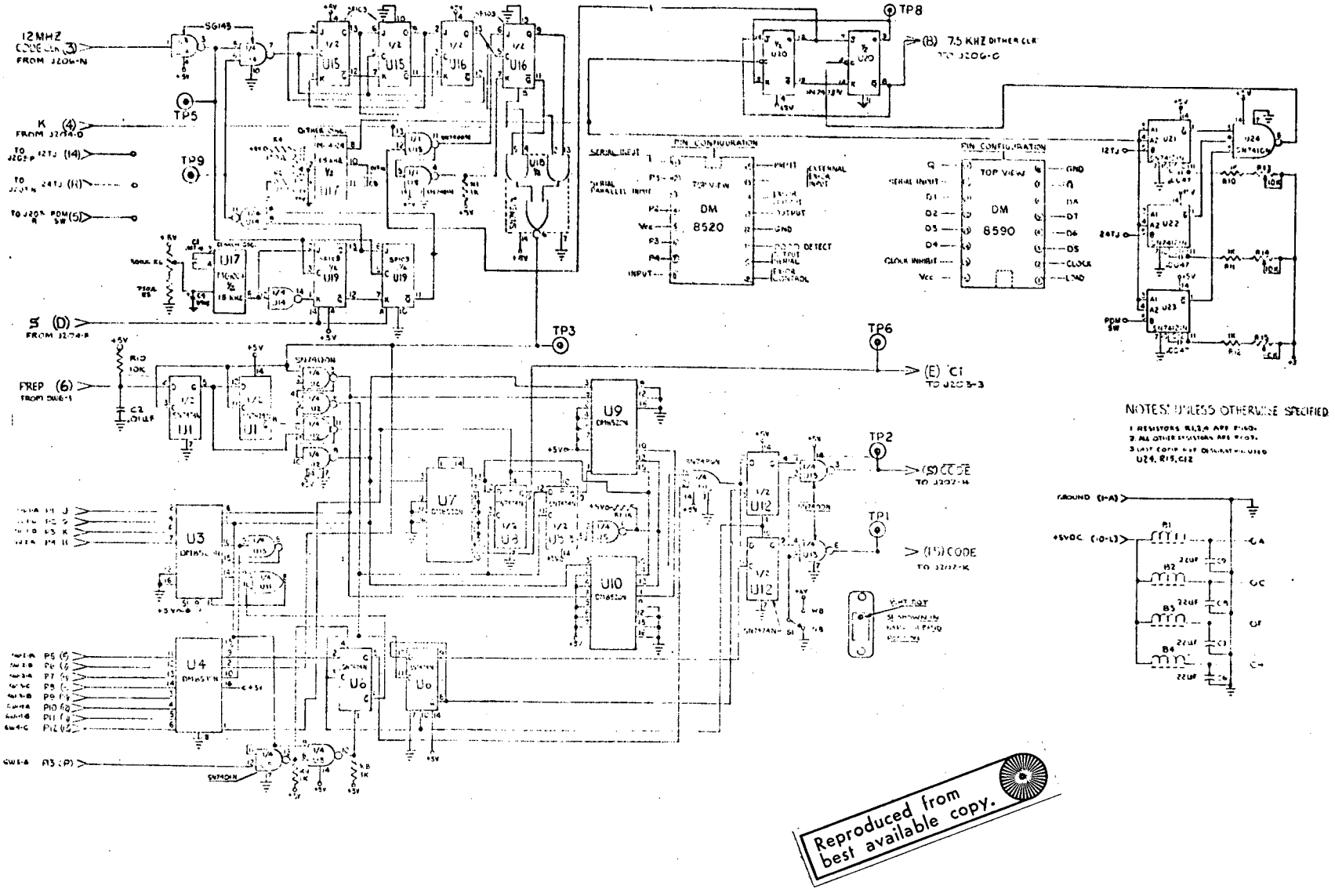
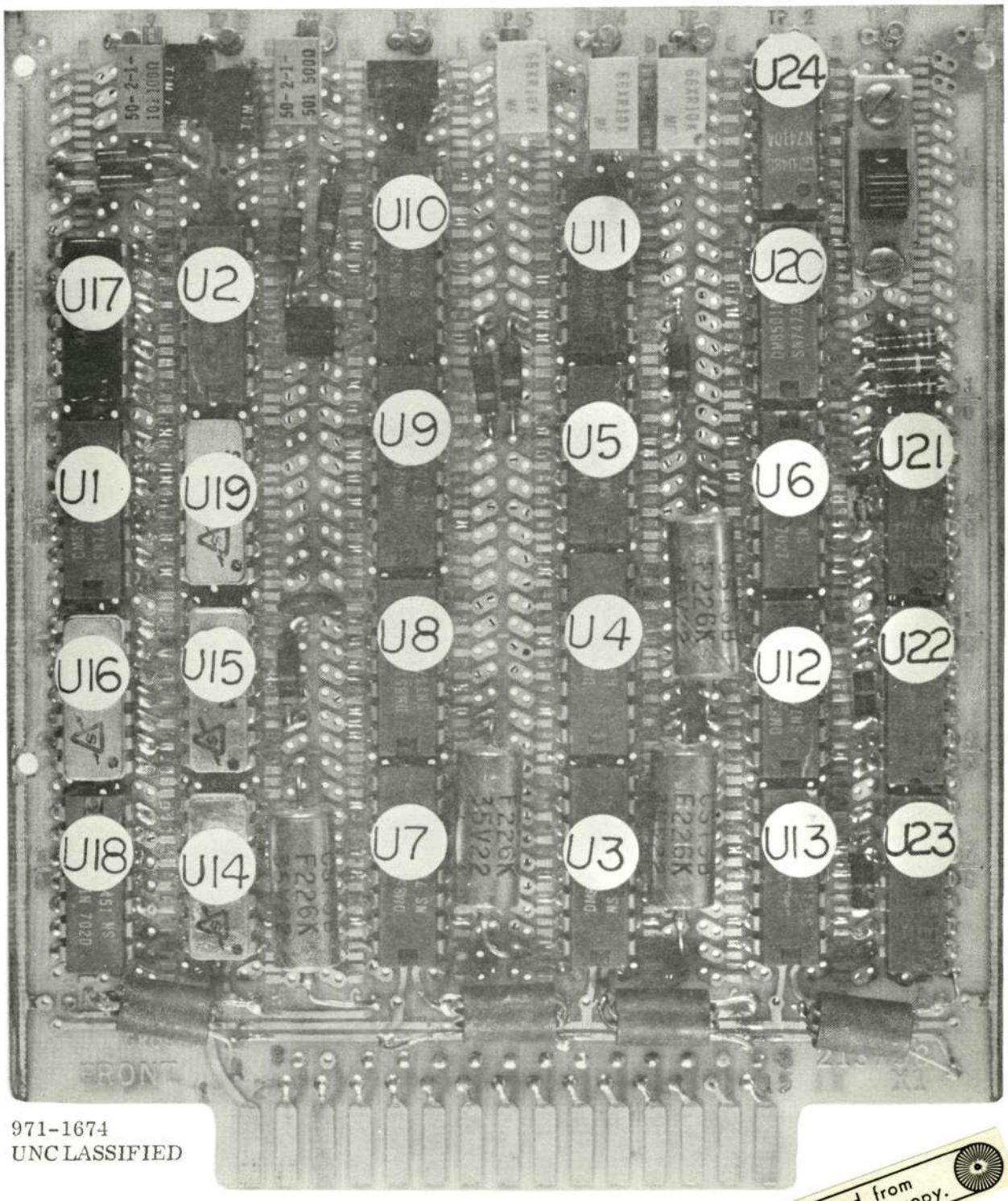


Figure 4-24. MX-291 Receiver J201 Coder Diagram Schematic



971-1674
UNCLASSIFIED

Figure 4-25. J201 Receiver Coder Board

c. Decode a run length vector (C_i) from one of the PNG's.

d. Perform the ± 0.2 bit shift on the coder clock at 7500 Hz rate when K signal is true.

e. Phase delay the coder clock in increments of 0.1 bit at a 15 kHz rate controlled by the S signal.

f. Phase the τ dither clock out to the clock board for the different data modes of operation.

Description of Implementation

Implementation of items a, b, and c above are covered under J102, the transmitter coder. Note that the 12 MHz coder input clock frequency is five times the PN coders clock rate. The receiver coder circuitry takes this five times clock rate and divides it by five to acquire the desired clock rate. From this divide-by-five network, five possible clock phases are always available, which are used to incremental phase shift (IPM) the coder clock. Also, if a signal 12 MHz clock pulse is inhibited, the coder clock would be phase shifted back by one fifth of a bit.

The τ dither process is used during the code tracking operations. To form the τ dither operation, the IPM property explained above is used. This is where the coder is phase shifted by plus and minus two tenths of a bit, or a total of two fifths of a bit, to generate the error signal of the coder clock tracking loop.

Before this system can code track, it must have code correlation, which means it must search out the code phase difference between the received code and the receiver's code. This unit accomplishes this operation by serial searching back to the transmitter phase (received code) in 0.1 bit increments. This search operation is implemented by using the previously explained incremental phase delay, by dropping a 12 MHz clock pulse. As stated, this shifts the receiver's coder clock back one fifth of a bit, which will result in a 0.1 bit delay in the 1.2 MHz Gold code. The objective of this system is to search through all phases, 8191 bits, of the Gold code in ten seconds. This means that 8191 12 MHz clock pulses per second on the average must be dropped to meet this requirement. S, the search command signal, gate controls the search oscillator. S is derived from the sync decision circuitry.

The sync decision circuitry has a false alarm rate of 30%. Therefore, the raw search rate must be increased to 1500 Hz to compensate for this condition. The raw search rate for this unit has been set to 1500 bps which requires a ten times rate at 12 MHz or a 15 kHz signal. This unit uses an IC (MC4024) oscillator for this signal.

The (MC4024) has two oscillators per package , so the other remaining oscillator is used for the τ dither operation and are set at 7500 Hz. The 7500 Hz dither rate is the same rate used by the MX-170B system; therefore, the τ dither demodulation network of this unit is the same as the MX-170B, (clock board).

IC one shot circuits were also used to form the delay required for phasing the τ dither clock to the clock board. A synchronous three-stage modified Johnson counter was used to form the divide-by-five network. The search, drop-a-bit process was accomplished by: (1) shifting the 7500 Hz search oscillator down a two bit register; (2) NAND gate the true side of the first register with the false side of the second register; (3) using this signal to inhibit the 12 MHz signal in to the divide-by-five counter.

The τ dither operation was implemented by mod-two gate selection of the required phase out of the Johnson counter with the 7500 Hz τ dither oscillator.

The formulation of the Gold codes in this unit MX-291 is the same circuit used by the MX-290 coder J102.

From figure 4-24, it is seen that:

a. U14-7 is the search drop-a-bit inhibit gate.

b. U17-6, U19, and U14 generate the inhibit pulse of one bit duration at a 7500 Hz raw rate. Note: (S) inhibits the two bit register.

c. U15 and U16 form the divide-by-five circuitry.

d. U17-8 and U20 form the τ dither control signal.

e. U18-6 is the mod-two operation of the τ dither gate.

f. U21, U23, U24-6, and U20-9 form the delay operation on the τ dither clock signal going to the clock board.

4.2.1.12 Multi-Mod J202

J202 is basically the same as J101. This board J202 has a TCXO set to 72 MHz where J101 has a VCTCXO set to 70 MHz. See figure 4-26 and 4-27.

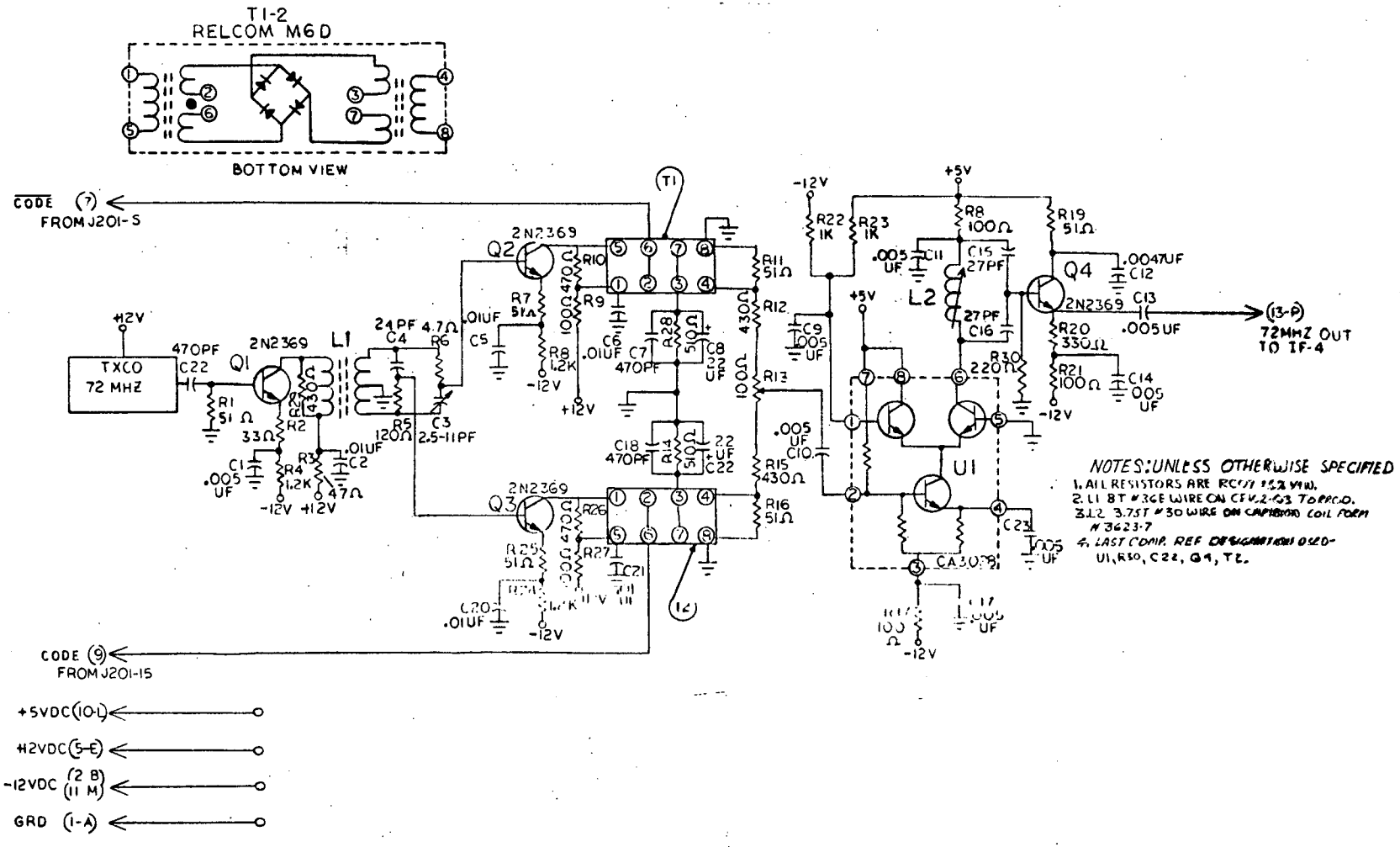
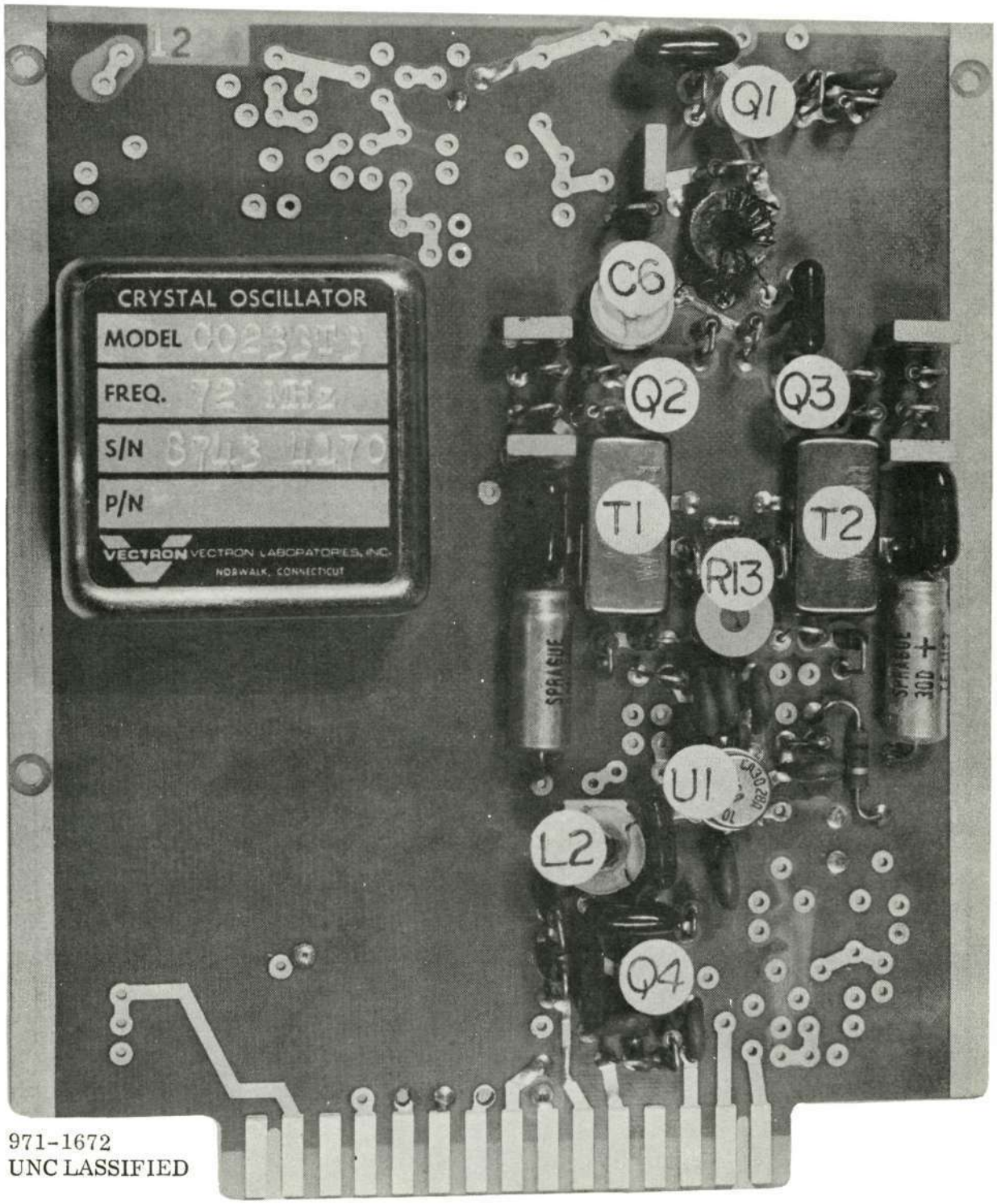


Figure 4-26. MX-291 Receiver J202 Multi-Mod Diagram Schematic



971-1672
UNCLASSIFIED

Figure 4-27. J202 Receiver Multi-Mod Board

Purpose

The purpose of J202 is to generate the 72 MHz PN signal.

Input/Output Routing

Referring to figure 4-25, note that this board has code and $\overline{\text{code}}$ as inputs, and the 72 MHz output as output. The code and $\overline{\text{code}}$ inputs come from J101. The 72 MHz output goes to the 70 MHz IF amplifier where it is used as the local reference input to the correlator.

Description

Refer to description of J101. Note: J202 has a 72 MHz TCXO, and the RF amplifier is not gate controlled.

4.2.1.13 Data (J203)

The following discussion of J203 is related to figures 4-28, 4-29, and 4-30.

Purpose

The purpose of J203 is to:

a. Convert the VCXO's 4 MHz sinusoid to a squarewave.

b. Generate the data clocks from the C_i signals.

c. Obtain the received digital data signal from $\_/\overline{I}$ and the required clock.

d. Interface to MIL-STD-188B the selected digital data clock and the received digital data when in the data mode.

e. Form the 12SBF and 24SBF signals.

Description of Implementation

The 4 MHz VCXO sinusoidal signal is converted to a squarewave by a 710 differential comparator. The data clocks are generated by multiplication of the C_i pulse via the phase lock loop method. The C_i phase is first divided by two to form a squarewave at 150 Hz. This 150 Hz signal is multiplied, via mod-two addition, with a 19.2 kHz oscillator divided down to 150 Hz. The signal out of the mod-two adder is filtered by a simple RC low pass filter, which is the loop filter. The loop filter drives an unijunction oscillator, which is divided by a binary counter chain to 150 Hz. The 9600 Hz, 2400 Hz and 1200 Hz clock signals are taken from the

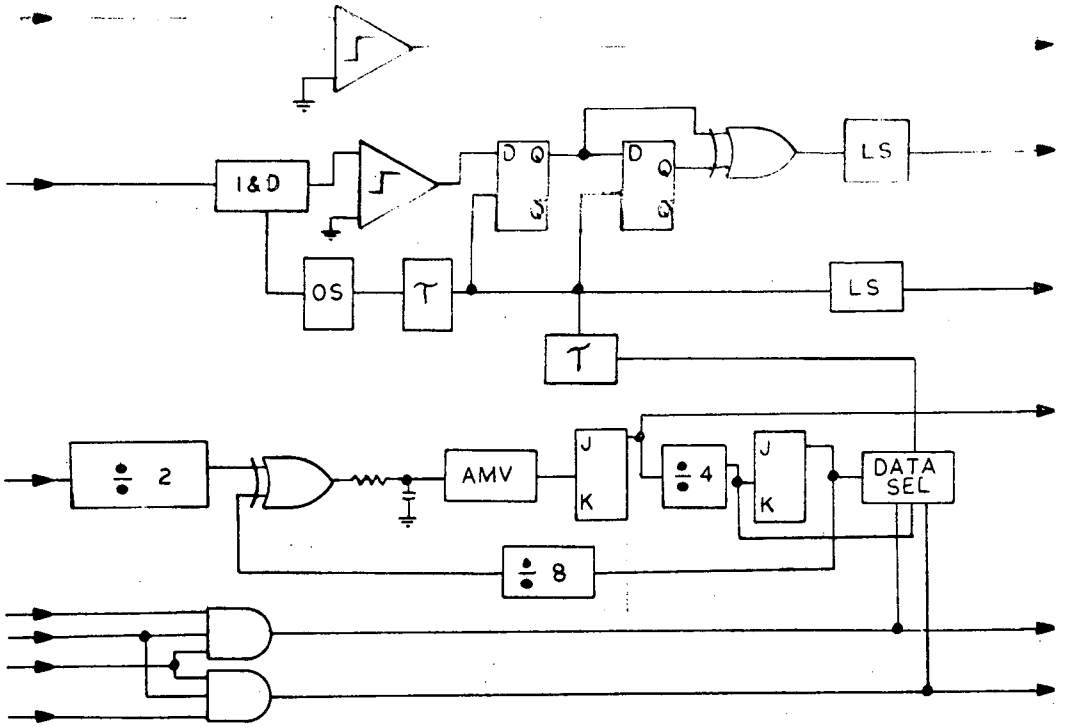


Figure 4-28. Data Board

appropriate flip-flop of the binary count down chain. The digital data clock signal is selected via a mod-two gate. The 2400 Hz or 1200 Hz signal from the PLL count-down chain is transferred out if the 24SBF or 12SBF respectively signal is true. The 2400 SBF signal is true if 24DR (the data rate switch is set to 2400), DATA switch, and K are all true. These signals, 24SBF and 12SBF, are simple AND gate operations. The circuits required to translate the TTL logic level signals to MIL-STD-188B consists of a OPA circuit, where the input network is a resistor and the feedback network is two back to back zener diodes. The greater than 5% rise and fall times were controlled by selection of the compensation caps.

The digital data decoding circuitry consists of: an I and D filter, followed by a Schmitt as the input to two D flip-flops in series and a clock used just prior to dump time, whose outputs are mod-two added to give the digital data signal. The integrator is a simple passive low pass RC circuit. The dump operation is accomplished by a fet switch circuit. The data Schmitt is a HA2625 OPA connected open loop non inverting into a common emitter amplifier circuit. The delay flip-flop are the 7400N series SN7474N or its equivalent. The delayed data clock dump after clocking into the D flip-flop pulse is generated by NAND gates and RC networks.

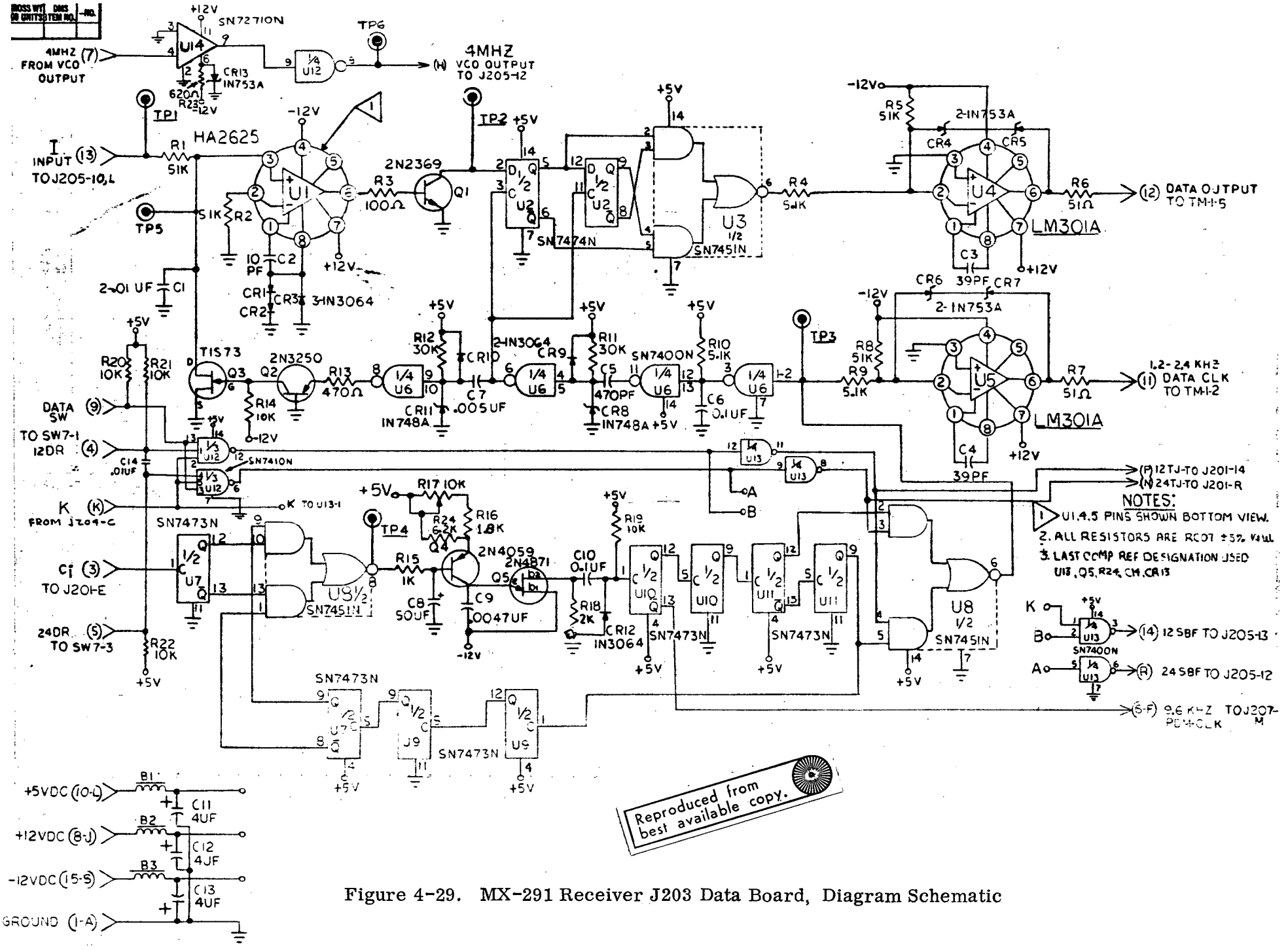
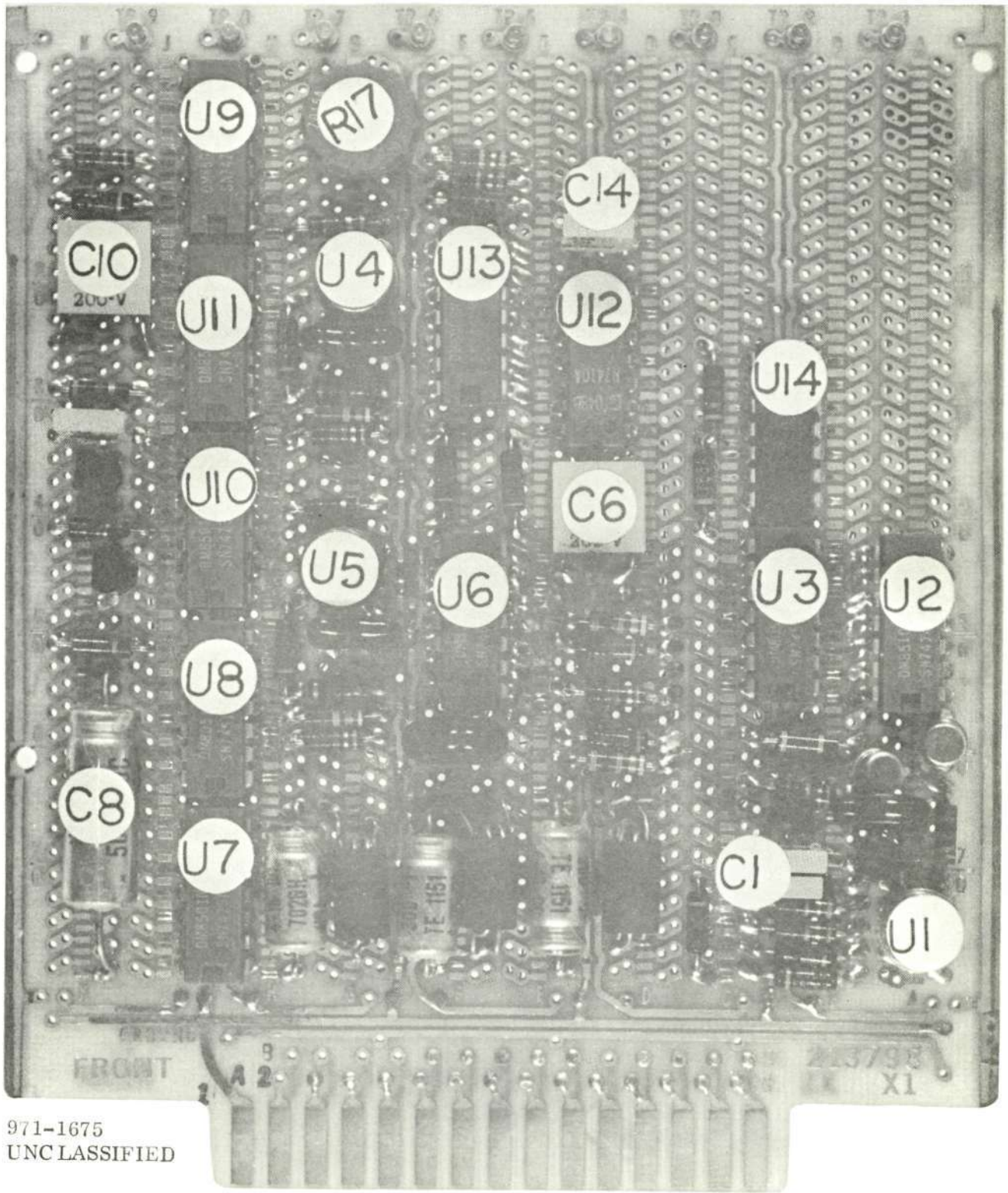


Figure 4-29. MX-291 Receiver J203 Data Board, Diagram Schematic



971-1675
UNCLASSIFIED

Figure 4-30. J203 Data Board

From figure 4-29, it is seen that:

a. The digital data integrator filter is R1 and C1.

b. The dump fet circuit consists of active elements Q3 and Q2.

c. The dump pulse, etc., network is formed by U6 and its associated passive element.

d. U2 is the digital data storate D flip-flops.

e. U3 is the mod-two adder required to decode the differentially encoded signals.

f. U4 is the active element in the network required to transfer the TTL level digital data to interface at MIL-STD-188B.

g. U7-12 divides C_i by two to form the 150 Hz squarewave.

h. R15 and C8 for the data PLL filter.

j. Q5 is the unijunction VCO for the data PLL.

k. U8-8, a mod-two adder, is the data PLL phase detector.

l. U7-9, U9, U10 and U11 form the binary countdown change of the data PLL.

m. U8-6 selects the digital data clock.

n. U12-12, U12-6, and U13 form the 24SBF and the 12SBF signals.

o. U14 and U12-8 Schmitt and buffer out the 4 MHz oscillator signal.

4.2.1.14 Controller (J204)

The following discussion of J204 is related to figures 4-31, 4-32, and 4-33.

Purpose

The purpose of J204 is to:

a. Generate the margin meter signal from $|Q|$.

b. Generate the AGC signals from $|Q|$ and/or $|I| - |Q|$.

c. Generate H and J sync decision signals from filtered $|I| + |Q|$.

d. Generate (S), the sync signal from H, J, and K.

e. Generate K, the final sync signal from filtered $|I|-|Q|$.

f. Generate the sync light signal from K.

Description of Implementation

The margin meter signal is formed by a 741 OPA inphase integrator. The $|I| - |Q|$ signal is formed by an OPA summer with $\overline{|I| + |Q|}$ and $|Q|$ as inputs. By giving $|Q|$ a weight of two and $\overline{|I| + |Q|}$ a weight of one the OPA summer output is $|I| - |Q|$. The $|Q|$ is also filtered to form the noise AGC signal. The $|I| - |Q|$

signal is filtered to form the signal AGC. The AGC amplifier will receive the most positive signal between the noise and signal AGC filter output. This is accomplished by emitter coupled emitter followers, see Q2 and Q3 of figure 4-32.The $|I| + |Q|$ signal is formed by the inversion of $\overline{|I| + |Q|}$ with a unity gain OPA inverter.

The $|I| + |Q|$ signal is AC coupled to a low pass RC filter to form the signal that the H Schmitt makes a hard decision on. H Schmitt has a fixed hysteresis and a variable off-set via a pot. The H Schmitt off-set is set so that H has a 30% false alarm.

The $|I| + |Q|$ signal is also low pass RC filtered to form the signal that J Schmitt makes a hard decision on. J Schmitt also has a fixed hysteresis and variable off-set via a pot. J Schmitt is adjusted so that it has a 10% false alarm rate.

The $|I| - |Q|$ signal is low pass RC filtered to form the signal that K Schmitt makes a hard decision on. K Schmitt is the final sync-lock decision circuit. Note that the Costas loop must also be in lock for K to make a decision. The H, J, and K Schmitt outputs are logically ORed to form the sync (S) signal. K is sent out

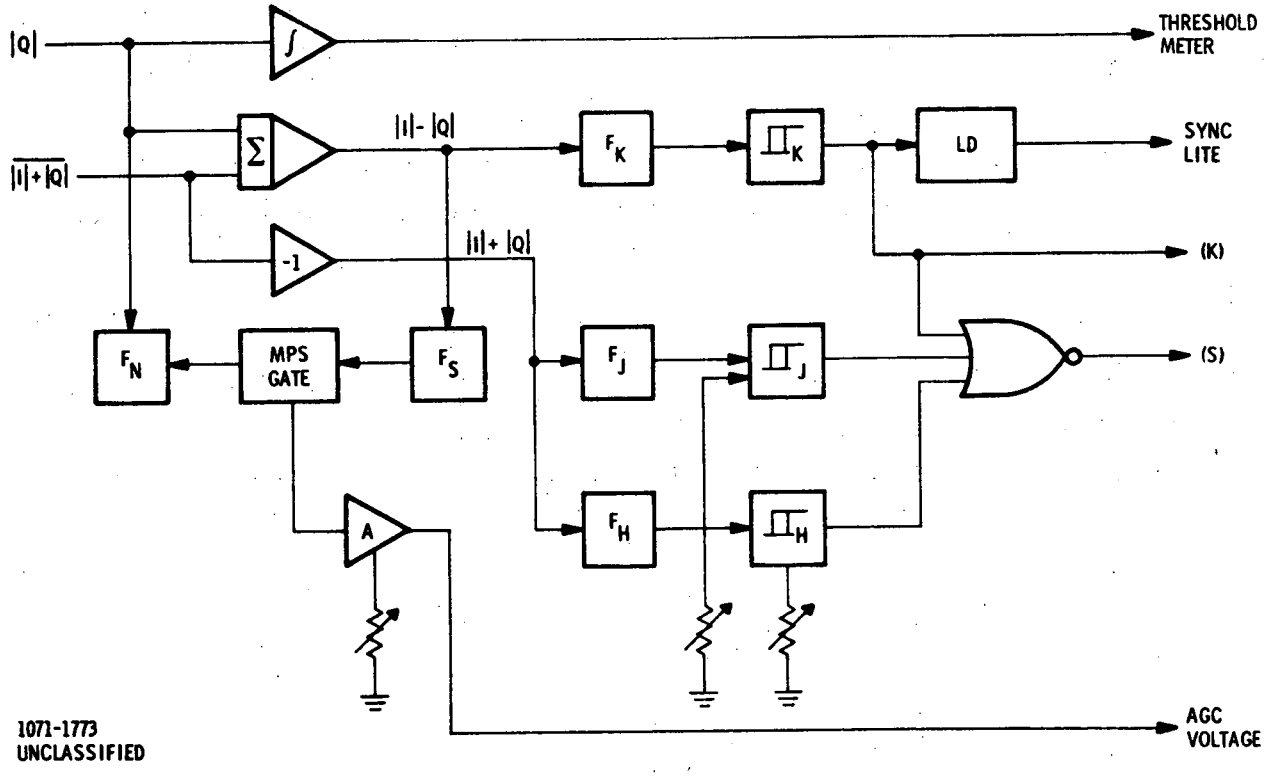


Figure 4-31. MX-291 Controller (J203) Block Diagram

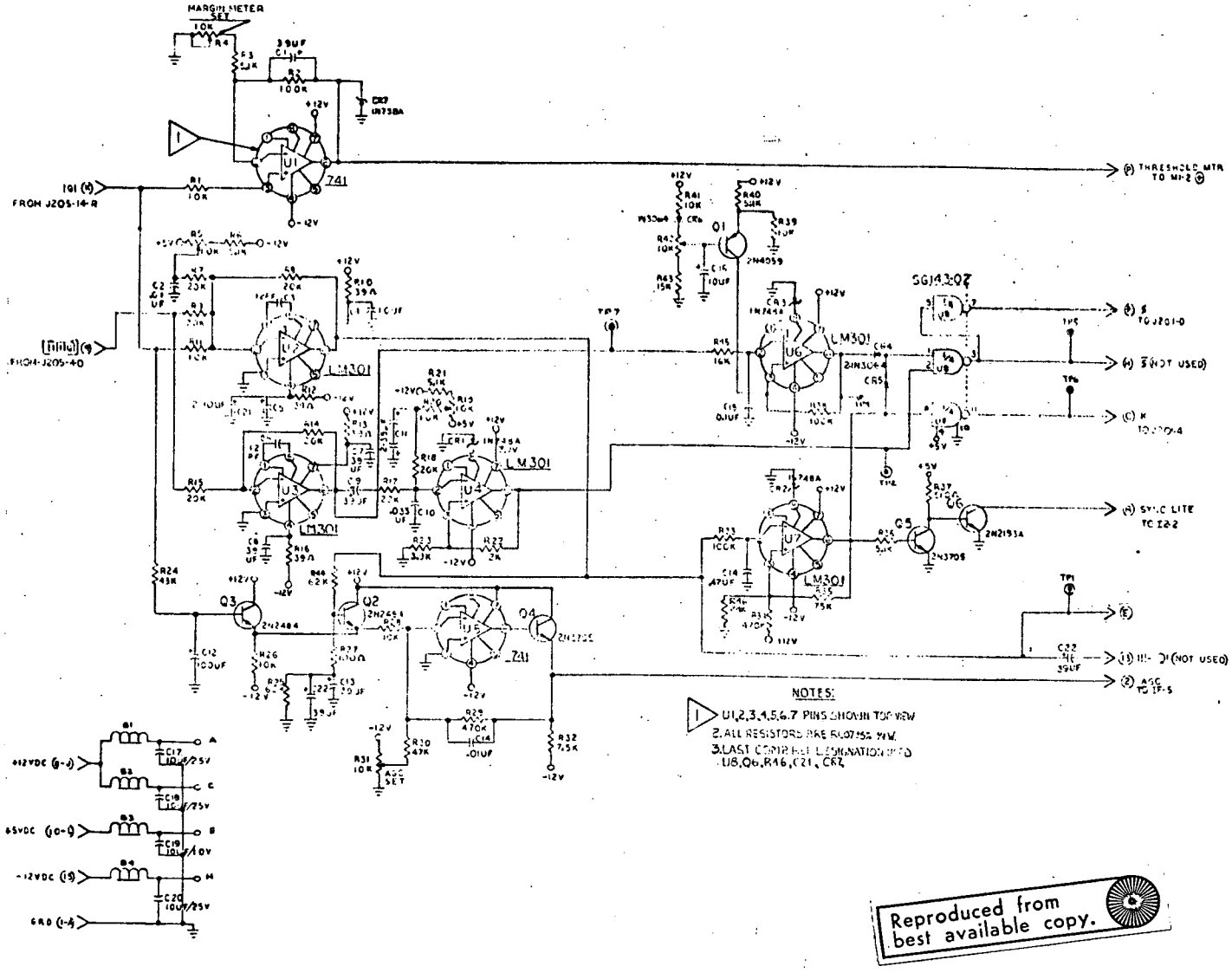


Figure 4-32. MX-291 Receiver Controller J204 Diagram Schematic

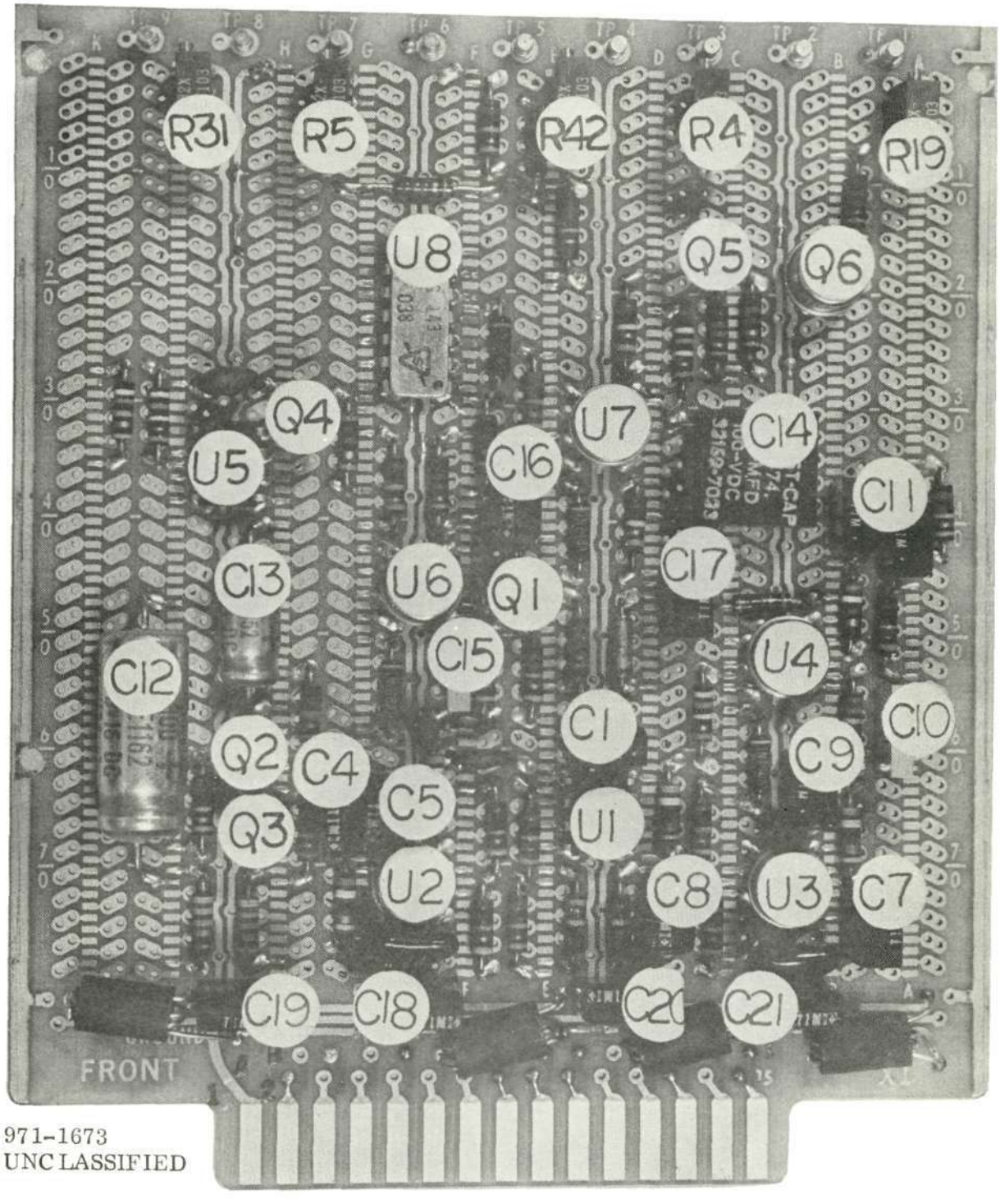


Figure 4-33. J204 Receiver Controller Board

as the final sync signal and is also the SYNC light signal.

From schematic figure 4-32, we can see that:

a. U1 is the non-inverting integrator required to form the margin meter signal from $|Q|$.

b. U2 forms $|I| - |Q|$ from $|Q|$ and $\overline{|I| + |Q|}$.

c. U3 forms $|I| + |Q|$ from $\overline{|I| + |Q|}$.

d. U4 is the H Schmitt.

e. U6 is the J Schmitt.

f. U7 is the K Schmitt.

g. U5 and U4 forms the AGC amplifier .

h. Q2 and Q3 forms the AGC signal selection most positive signal gate.

4.2.1.15 Digital Receiver J205

The following discussion refers to figures 4-34, 4-35, and 4-36. The digital receiver card J105 is a post correlation receiver that synchronously demodulates and tracks the carrier via a Costas loop technique. The purpose of J105 with its VCXO that is mounted on a plate above the + 5 volt power supply is to:

Purpose

a. Extract the inphase vector $|I|$ and the quadrature vector $|Q|$ of the post correlator signal.

b. Generate the magnitude of $|I|$ symbolically $|I|$ $|Q|$.

c. Generate the magnitude of $|Q|$, symbolically $|Q|$.

d. Generate the hard decision value of I called Schmitted I and ($\_/\overline{I}$).

e. Form the sum of I magnitude, $|I|$, and Q magnitude, $|Q|$symbolically.

Inputs/Outputs

The 2 MHz input comes from the 70 MHz RF amplifier via subminature coat. The 4 MHz VCXO input is from the data board J203. The data board converts the 4 MHz sinusoid of the 4 MHz VCXO to a squarewave. The 12SBF and 24SBF inputs come from the data board. Input K, the final sync decision command, comes from J204. The $|I|$, $|I| + |Q|$, and $|Q|$ all go to J204. The $|I|$ also goes to J203.

Description of Implementation

The 2 MHz input signal is first amplified by a factor of ten (20 dB). This amplifies also restricts the signal bandwidth down to a 3 dB bandwidth of 42 MHz.

Note, this sets the noise level into the Costas loop multipliers. This amplfier's output signal is a KEY VALUE which is set to one volt peak-to-peak when the system is in sync and the Costas loop is in lock. This one volt peak-to-peak signal level sets the gain constant of the detector in the Costas loop. Remember also that derivatives of this signal are used to obtain data and clock tracking signals. Also, note the DC coupling conditions from the input of the loop multiplier out through $|I|$, $|Q|$, I, Q, $|I| + |Q|$ and the VCXO control signal line. To summarize, this one volt signal most important because it enters the I and Q multipliers where it is multiplied by the inphase or quardature component of the 2 MHz carrier reference signal. I and Q signals result from this multiplication. Each I and Q signal are then filtered by their sideband filter. This unit has three sideband filters (SBF) 1200 Hz, 2400 Hz and 9600 Hz. When the MX-291 is in the search mode, the 1200 Hz SBF is used.

When in the tracking mode, the 1200 Hz, 2400 Hz, or the 1200 Hz filter is used for the voice, 2400 bps data rate or 1200 bps data rate mode, respectively.

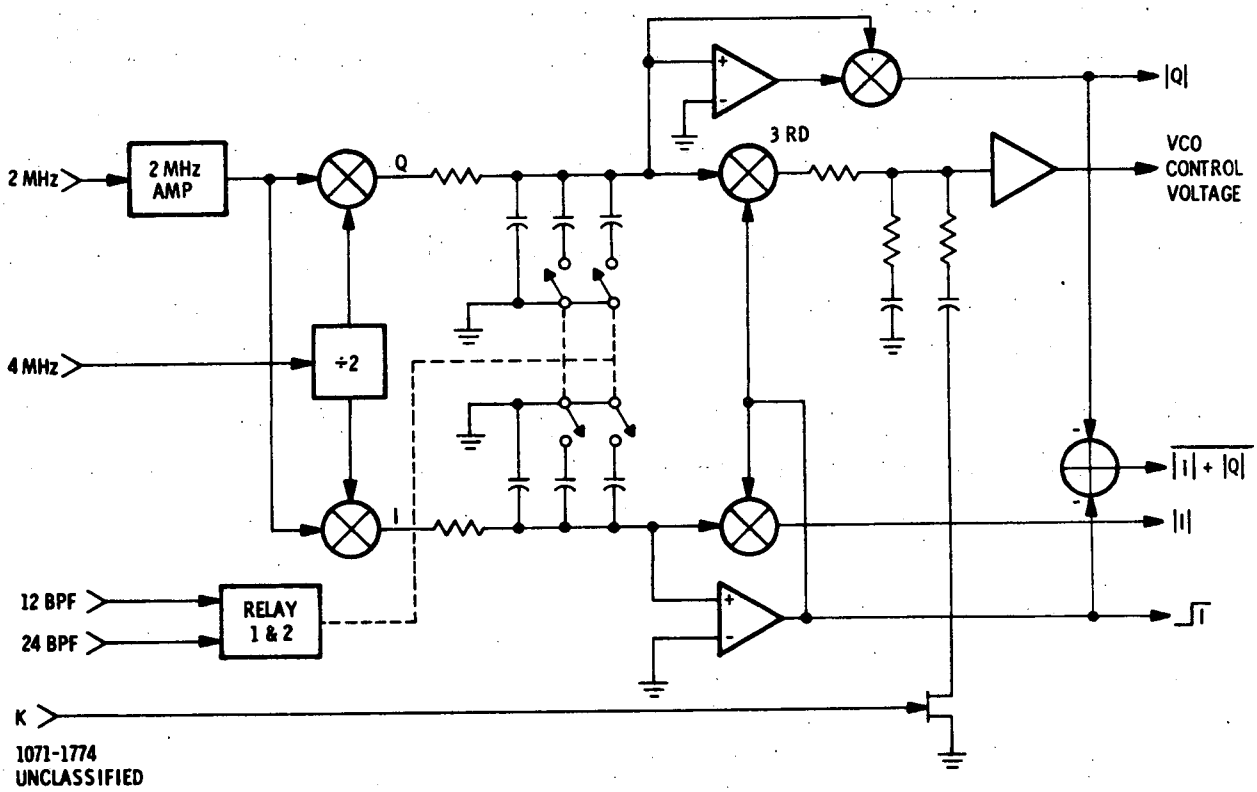


Figure 4-34. Digital Receiver J205 Block Diagram

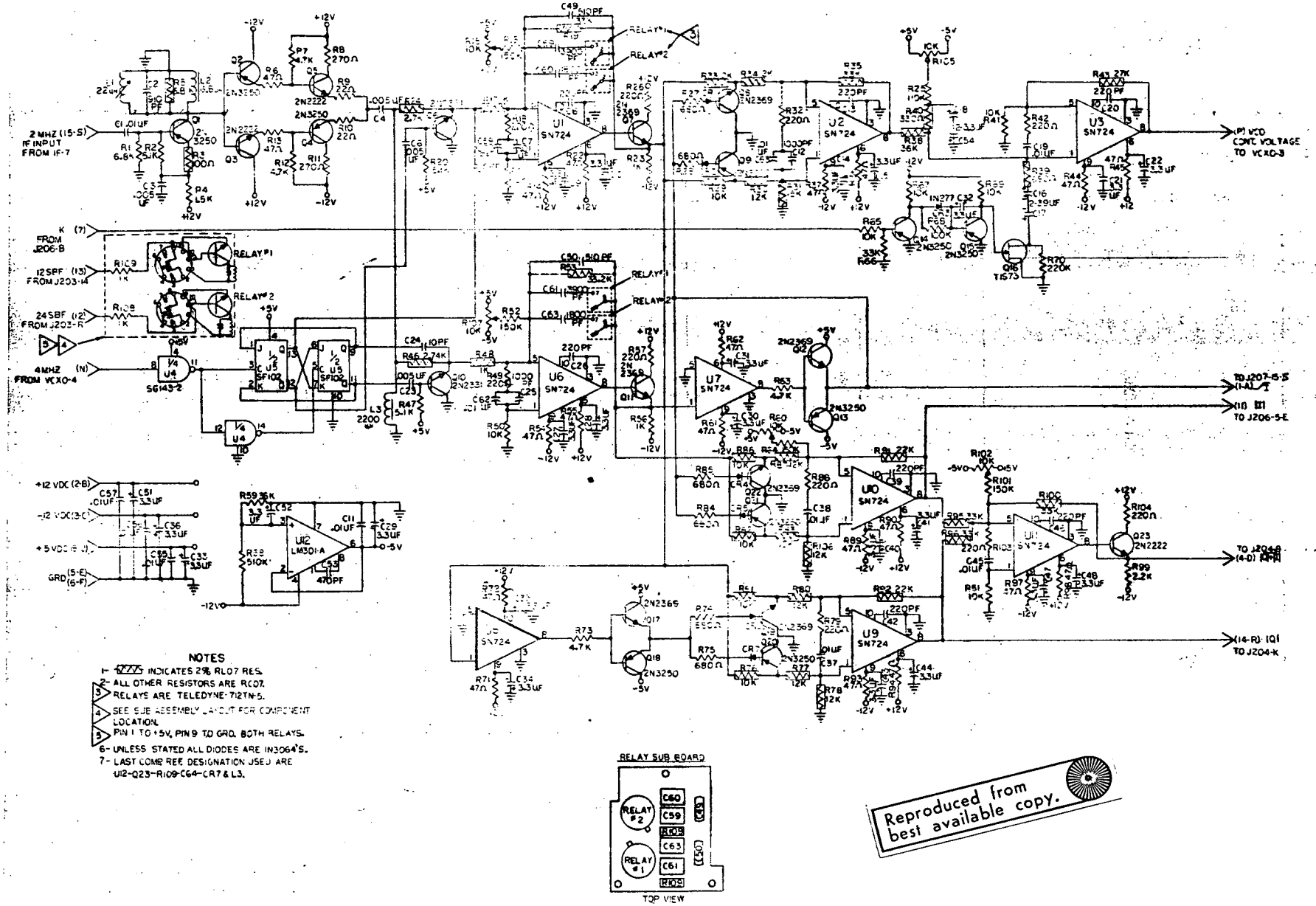
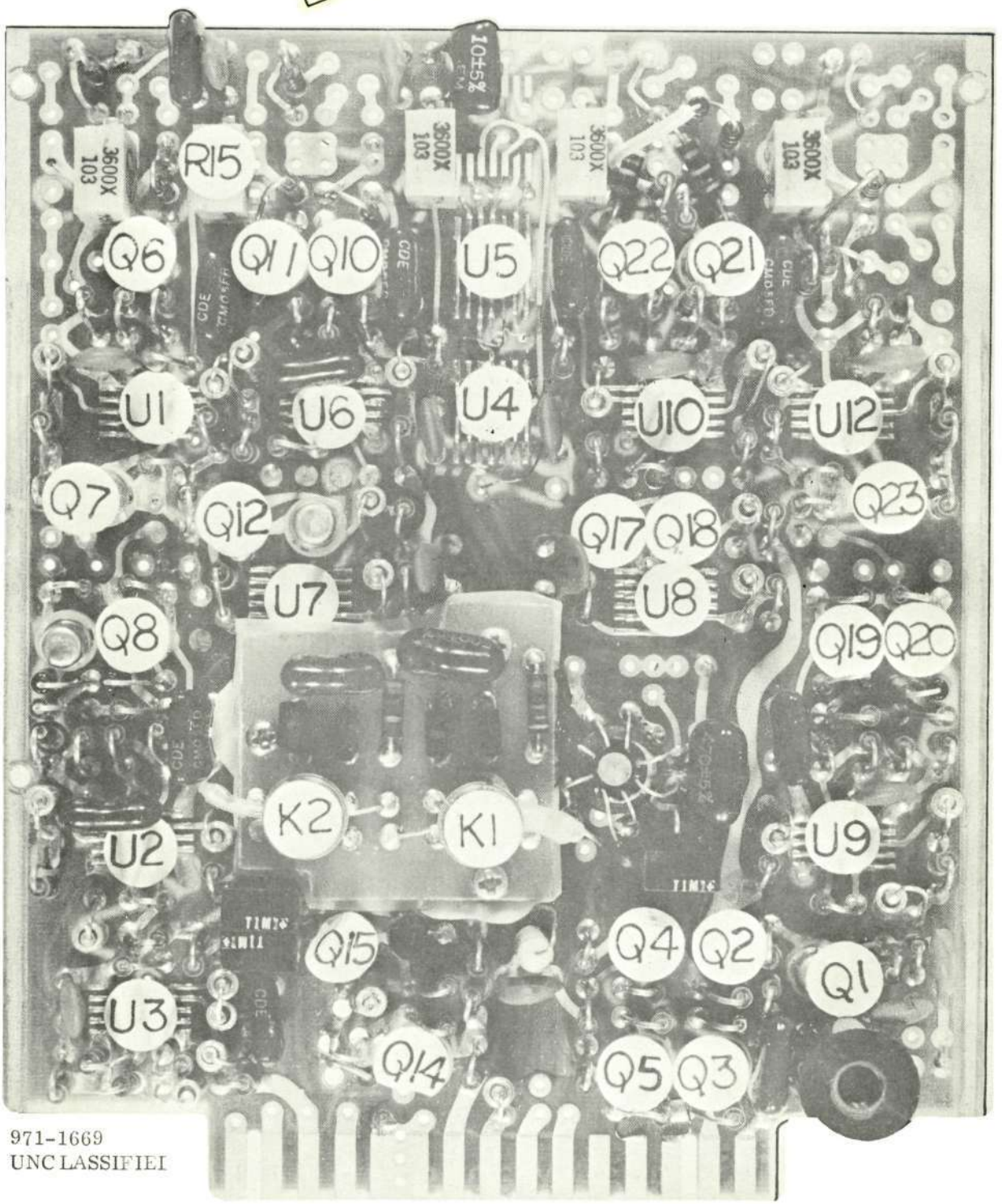


Figure 4-35. MX-291 Digital Receiver Board J205 Diagram Schematic



971-1669
UNCLASSIFIED

Figure 4-36. J205 Digital Receiver Board

This filtered output from I and Q is each Schmitted and transferred out as Schmitted I ($\_/\overline{I}$) or Schmitted Q ($\_/\overline{Q}$). The Schmitted I is used as the LO for magnitude of I ($\_/\overline{I}$) mixer and the third multiplier of the Costas loop. The $\_/Q$ signal is multiplied with Q to obtain |Q| signal. |Q| and I signals are found are found on pins 14-R and 11. Also, |I| and |Q| are summed by an OPA to form inverted sum of |I| and |Q|, (|I| + |Q|). The Costas loop third multiplier output, the product of I and Q, is filtered by the selected loop filter, acquisition or track. The acquisition filter is used during acquisition and the tracking filter during tracking mode.

The loop filters are passive proportional plus, with the series resistor being common. The tracking filters shunt elements (R and C) are gated in by a fet switch activated by K, the final sync decision signal. The acquisition filters shunt elements are not removed when K occurs, but are considered as part of tracking filter.

The loop filters output is buffer-amplified by 5.7 dB and sent out as the Costas loop VCXO's control voltage. The 4 MHz VCXO is mounted on a plate aside the + 5 volts power supply. The VCXO sinusoid output is first Schmitted by a 710 differential comparator located on the data board, then transferred to J205. This squarewave 4 MHz VCXO input signal to J205 is connected to a modified Johnson counter. The Johnson counter outputs generate the reference I and reference Q signals for the I and Q multipliers.

The 2 MHz, 42 kHz bandpass, buffer-amplifier consists of active elements Q1, Q2, Q3, Q4, and Q5. The Q channel multiplier and sideband filter network consists of active elements Q6, U1, and Q7. The I channel multiplier and sideband filter network consists of Q10, U6, and Q11. U7 Schmitts I and Q12 and Q13 buffier $\_/\overline{I}$. U8 Schmitts Q and Q17 and Q18 buffer $\_/\overline{Q}$. U9, Q19 and Q20 form |Q|, and U10, Q21 and Q22 for| I |. U11 and Q23 sums and inverts |I| and |Q| to form the $\overline{|I| + |Q|}$ signal. U2, Q8 and Q9 is the third multiplier. R38 is the common series element of the acquisition and task filters. R40, C18, and C54 form the shunt leg of the acquisition filter. R39, C16, and C17 form the shunt leg of the tracking filter. Q14, Q15, and fet Q16 are the active elements of the loop filter gate. U3 is the loop buffer-amplifier. U12 is used to form a -5 volt supply on this board.

4.2.1.16 Clock Board J206

The following discussion refer to figure 4-37, 4-38, and 4-39.

Purpose

The purpose of J206 is to extract the coder clock error control signal from the I signal, filter and use it to control the coder clock VCO on this board.

Inputs/Outputs

|I|, K, and 7.5 kHz dither CLK are the input signals with the 12.2865 MHz code clock as the output. Input |I|, which is the absolute magnitude of the inphase signal of the Costas loop, comes from J205. Input K, the final sync decision signal, comes from J204. The 7.5 kHz dither CLK input signal, comes from J203. The 12 MHz code CLK output is the clock signal for the coder, an it goes to J201.

Description of Implementation

The |I| signal is first filtered by an active BPF (two pole, one zero) filter. This filter is centered at the 7.5 kHz dither frequency, with a 3 dB bandwidth of 450 Hz. This filtered signal is then mixed or multiplied with the 7.5 kHz dither CLK, which is the phase detector of the coder clock tracking loop. The 7.5 kHz dither CLK is gated only after the K signal occurs. This is accomplished by a digital logic NAND gate. The output of the phase detector is then filtered by the loop filter, which is an active proportional plus. The output of the loop filter is then applied to the coder clock VCO. The coder clock output goes to the coder board.

From figure 4-38, it is seen that:

a. The active BPF consists of U1 and its associated passive components.

b. U2, Q1, Q2, Q3, and Q4 are the active components of the multiplier or phase detector.

d. U3 is the active element in the loop filter.

e. The 12 MHz VCXO is the Vectron oscillator on the board

f. NAND gate U4 is the 7.5 kHz, K gate operation.

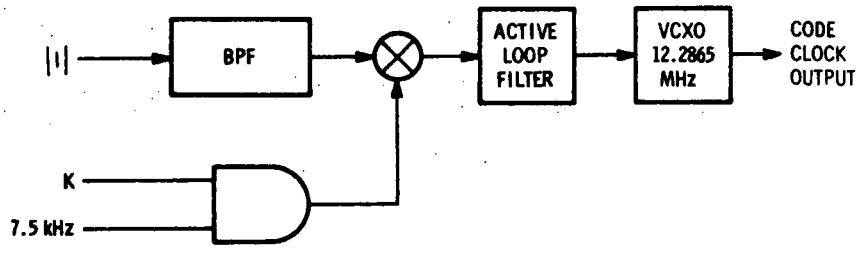


Figure 4-37. Clock Board J206 Block Diagram

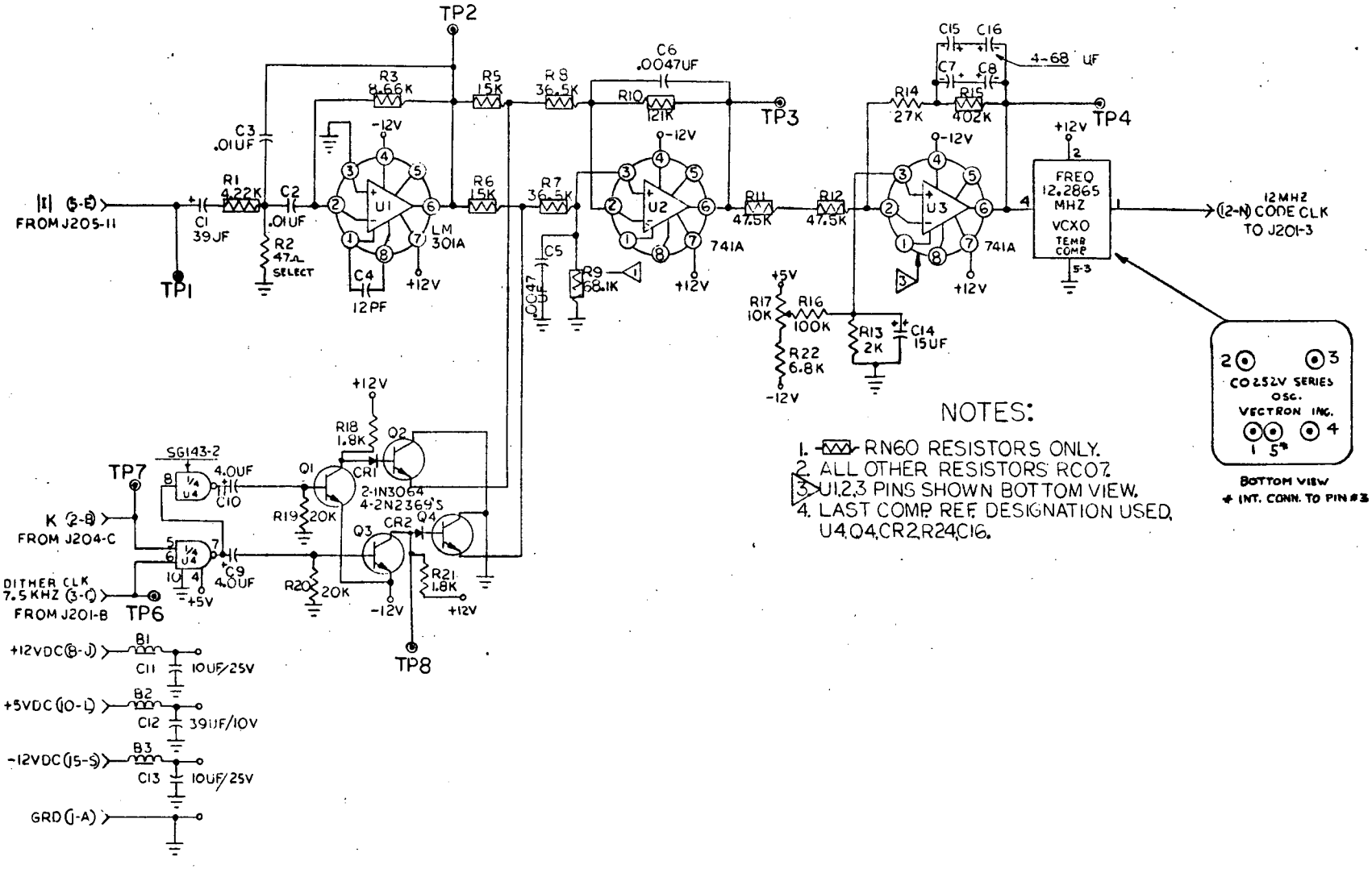


Figure 4-38. MX-291 Clock Board Receiver J206, Diagram Schematic

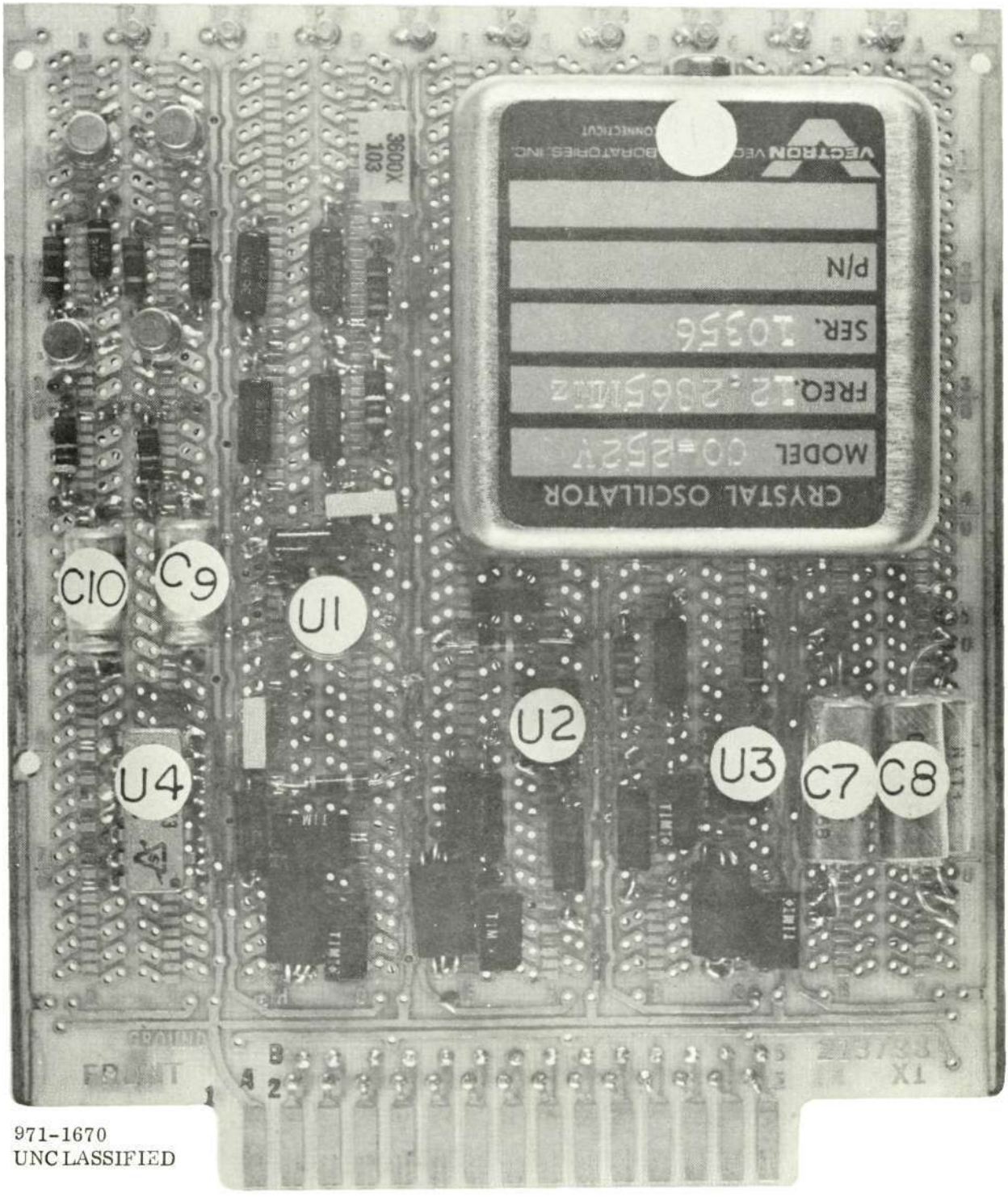


Figure 4-39. J206 Receiver Clock Board

The following discussion is given to extend insight on implementation, and is not essential for basic conceptional understanding of hardware.

A simplified steady state, etc., expression of the voltage transfer function of the BPF in polar form is:

$$\frac{e_0\,(S)}{e_{in}\,(S)} = \frac{-S/R1C3}{S^2 + S\,(1/(C2C3R3[C2 + C3]) + R1\,R2/(C2C3R3[C2 + C3])}$$

where the components callout is from SK42-006. Note, that by varying R2 only Wn is changed. Also, C2 = C3, therefore, Q = R3/4R2 and center frequency gain A = R3/2R1. Inserting the given component values Q = 20 and A = 10.

From the above information, we can consider the filter as a simple RCL circuit where a series RC is connected between the input and output ports with the L shunting the output port. The values are selected so that the undamped resonant frequency is 7500 Hz and the circuit Q is 20.

The simplified voltage transfer function of the coder clock active loop filter in time constant form is:

$$\frac{e_0\,(S)}{e_{in}\,(S)} = \frac{-(_{14} + R_{15})\;(SC_7\,R_{14} + 1)}{(R_{11} + R_{12})\;(SC_7\,R_{15} + 1)}$$

where the component callout is from figure 4-38 and the parallel equivalent of R14 and R15 is R14.

From the above equation, its zero is located at $1/(C_7R_{14})$ and its pole is at $1/(C_7R_{15})$, which are real roots on the sigma axis of the S plan. Also, the ratio of the zero to the pole is the ratio of R_{15} to R_{15}.

Now, consider the simplified open loop transfer function of the coder's clock tracking loop. This would be the above roots and one pole at the origin for the VCO. By constructing the root locus from the open loop transfer function, all values of K, the gain, are observable. Remember that the root locus plot is the logic of points for all values of gain. From this root locus, we can see how the closed loop roots vary, as gain varies. The gain K, of this loop, is dependent upon signal to noise ratio during the acquisition to track mode transistion. To simplify analysis normalize to the real pole, hence, the zero is located at R_{15}/R_{14}.

4.2.1.17 PDM - Receiver Processor (J207)

As seen from figures 4-40, 4-41, and 4-42, the PDM receiver processor is a relatively simple operation. The Schmitted inphase conponent, $\overline{I}$, of the post correlated signal is mod-two added with the PDM clock to form the PDM signal. This PDM signal is first converted to a PAM signal, then deemphasized, and low pass filtered to form the audio output signal. This audio output signal goes to the external speaker and its driver circuit. The SCPDM demodulator processor and the 2500 Hz LPF are thick film circuits.

The $\overline{I}$ signal is converted to TTL level by Q1 as seen in figure 4-41. U2 converts the SCPDM signal to the unfiltered audio signal. U3 is the thick film, 2500 Hz, ODB gain, active filter. This is the same filter used by the transmitted SCPDM processor. The 9600 Hz clock is buffered by U1-8, and U11. The U1-3 and U16 form an inhibit signal consisting of K and PDM SW. This signal inhibits or squelches audio output until the PDM mode has been selected and the system has acquired the K signal (sync and lock).

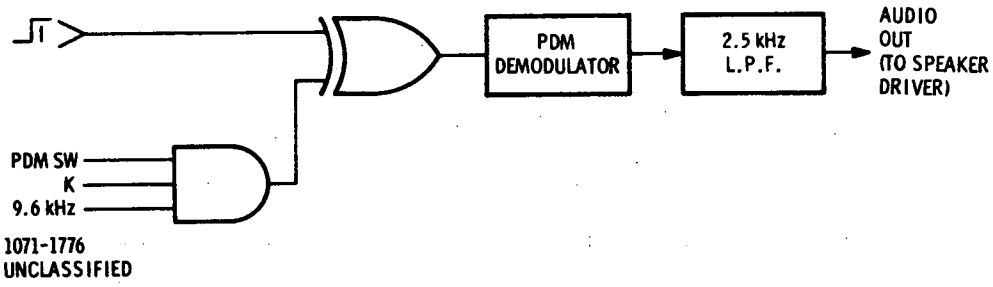
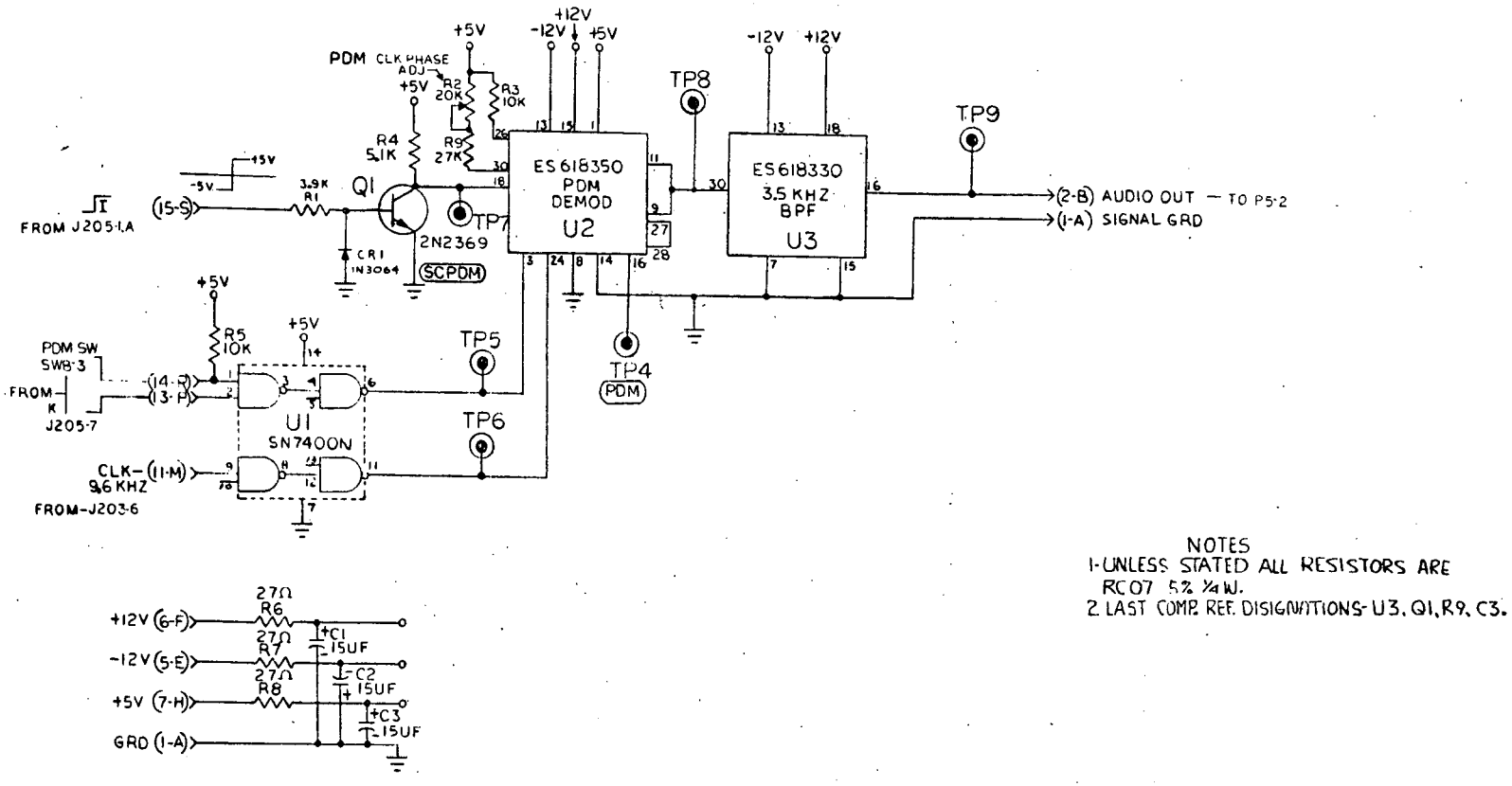
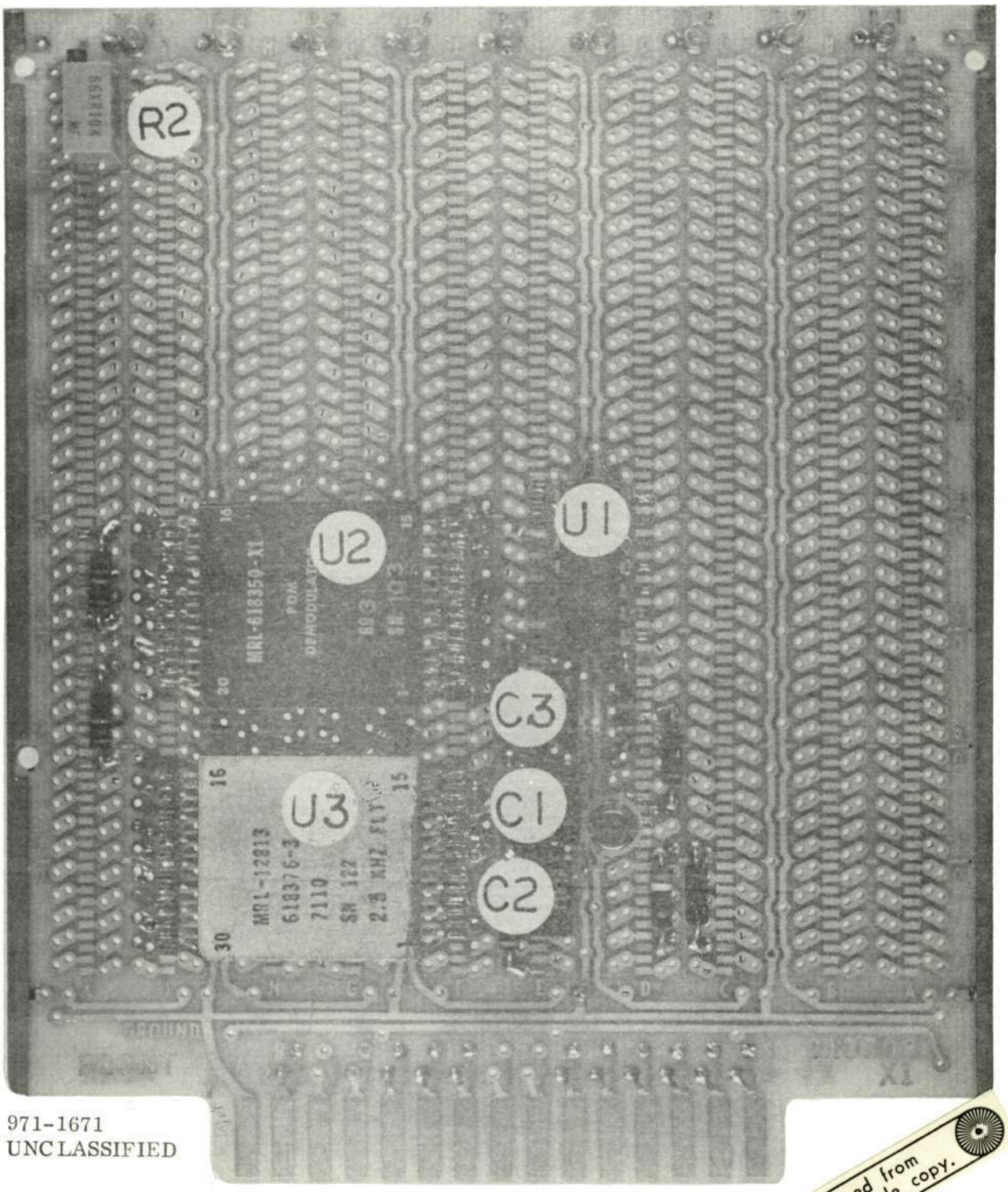


Figure 4-40. PDM Receiver Processor (J207) Block Diagram



NOTES
1-UNLESS STATED ALL RESISTORS ARE RC07 5% ¼W.
2 LAST COMP REF DISIGNATIONS-U3, Q1, R9, C3.

Figure 4-41. MX-291 PDM Receiver Processor J207 Diagram Schematic



971-1671
UNCLASSIFIED

Figure 4-42. J207 PDM Demod.

4.2.2 CHASSIS PHYSICAL LAYOUT

The overall dimensions of the receiver unit are the same as those of the transmitter unit, namely, 9 x 7 x 13 inches. The physical location of the various components of the receiver unit are shown in figure 4-42. Some of the internal adjustments are also shown.

4.2.3 SINGLE LOCATION AND FLOW CHARTS

A number of test points useful for maintaining and servicing the receiver unit are available both on top of the cards and on the connector pins accessable from the bottom of the chassis. Figure 4-43 shows the location of the test points and the designation of the corresponding signals. Simply, figure 4-44 shows locations of the various signals on the card connectors. Figure 4-45 shows the signal flow on a card-to-card basis. Refer to Appendix A for explaination or definitions of symbols.

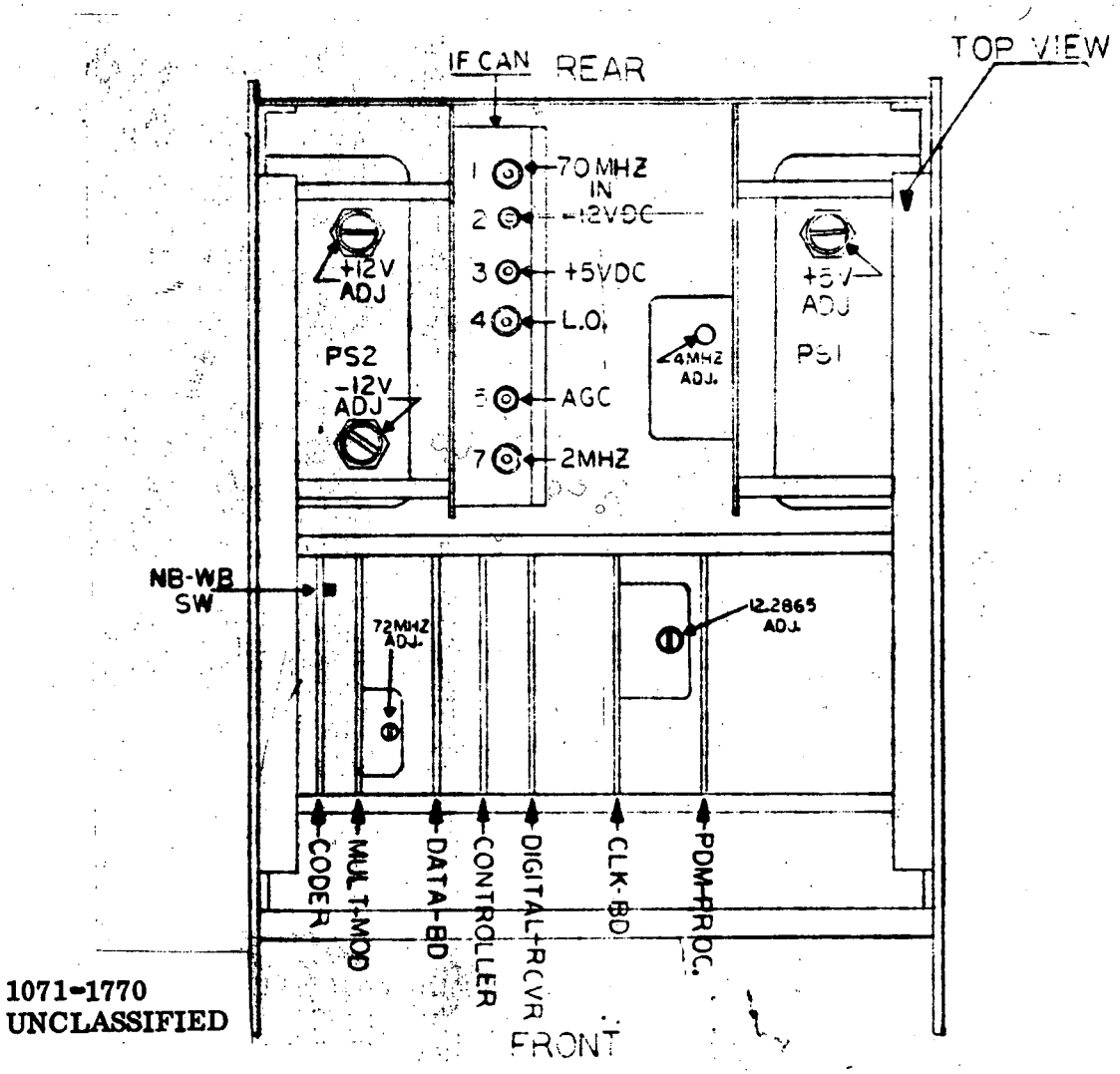


Figure 4-43. MX-291 Component Location

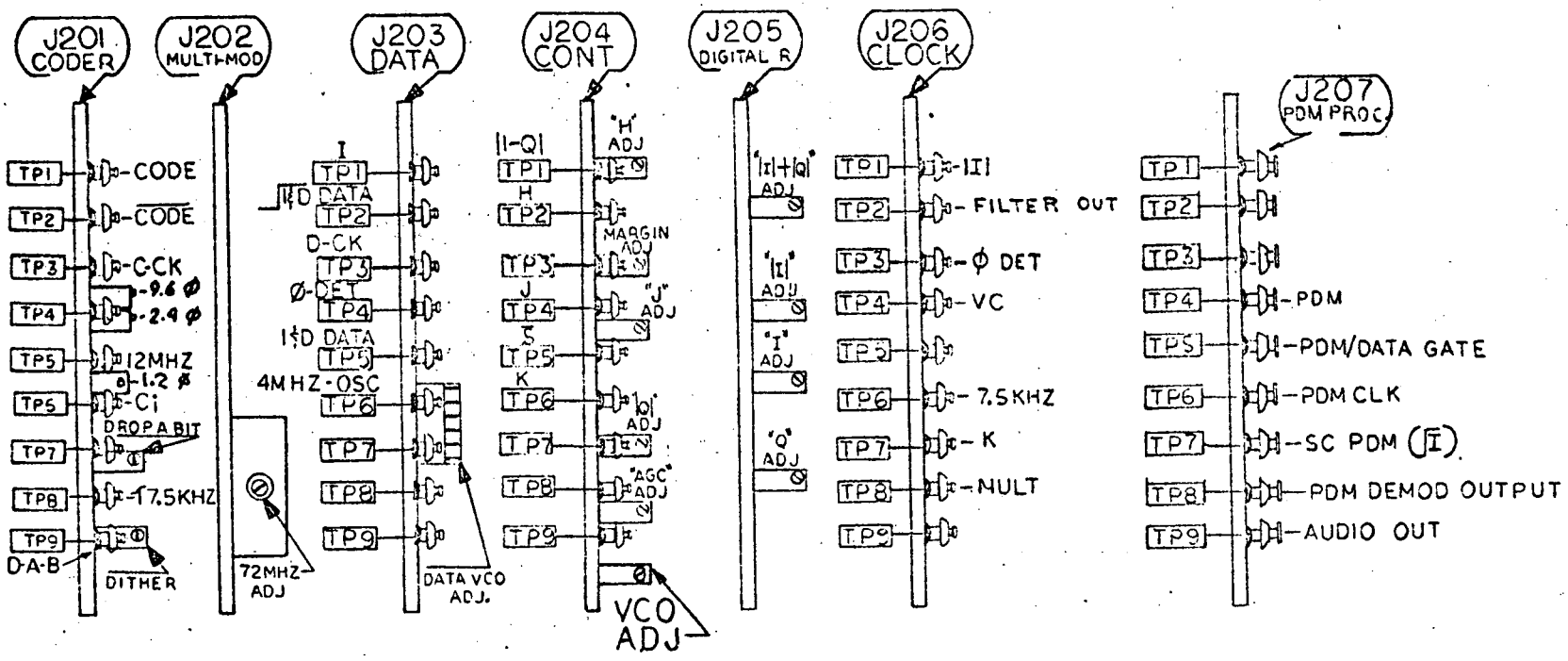


Figure 4-44. MX-291 Receiver Test Points and Adj.

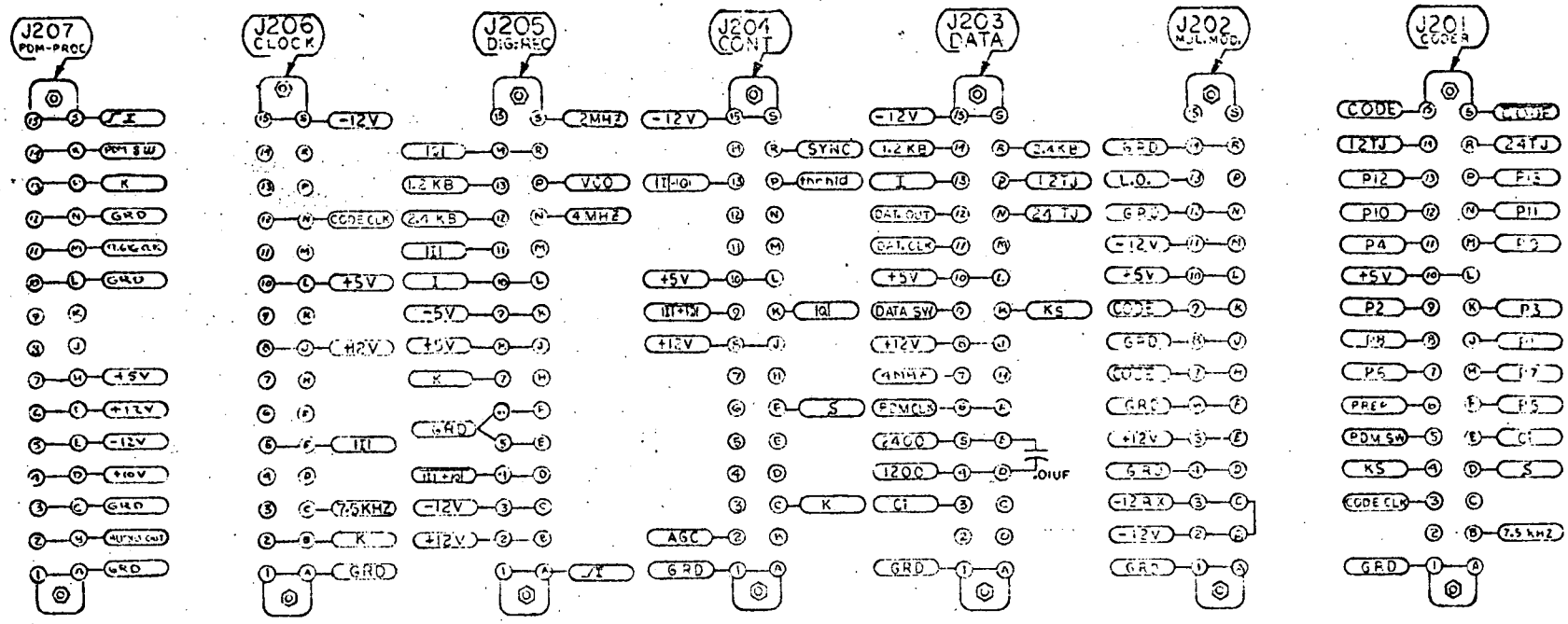


Figure 4-45. MX-291 Receiver Function Symbol Location Diagram

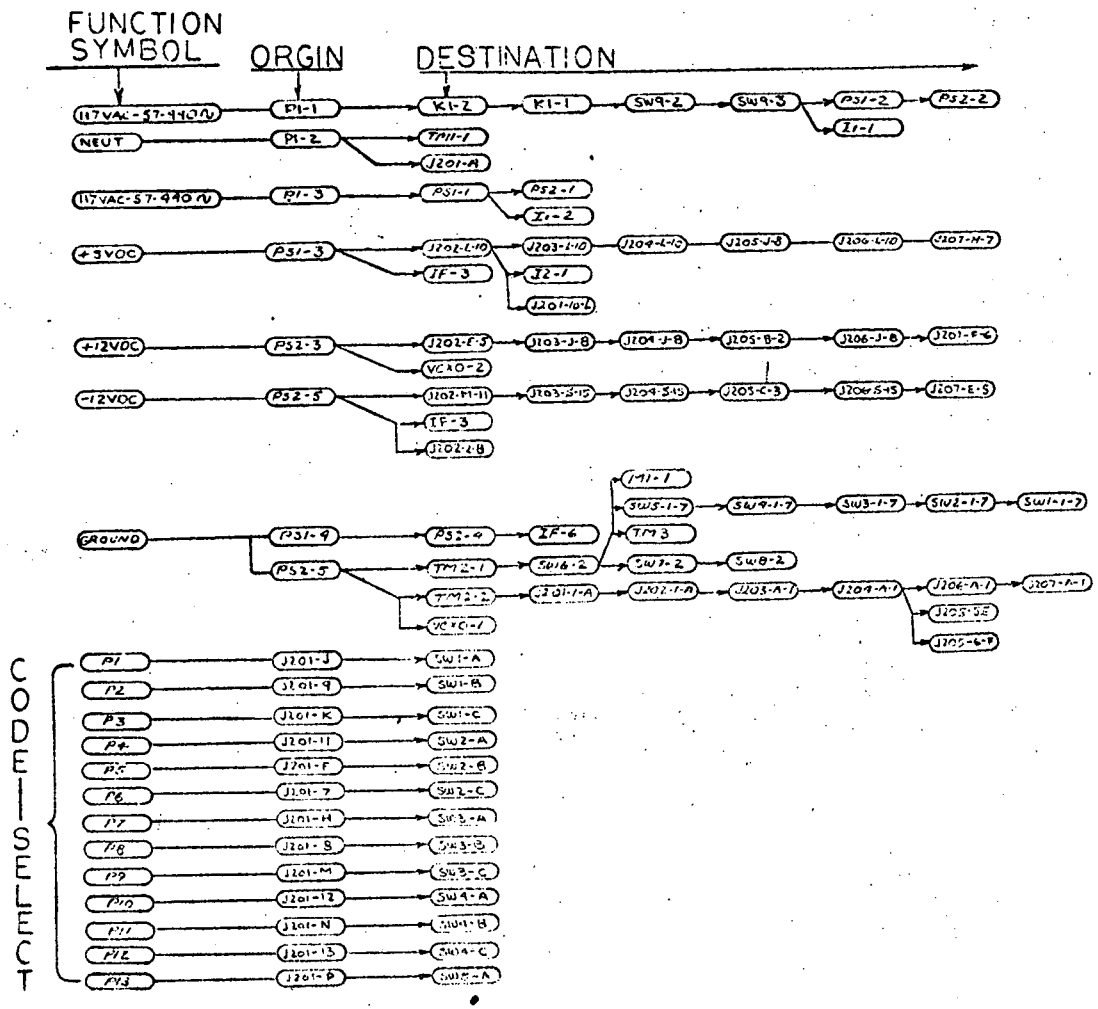


Figure 4-46. MX-291 Function Symbol Routing Diagram. (Sheet 1 of 2)

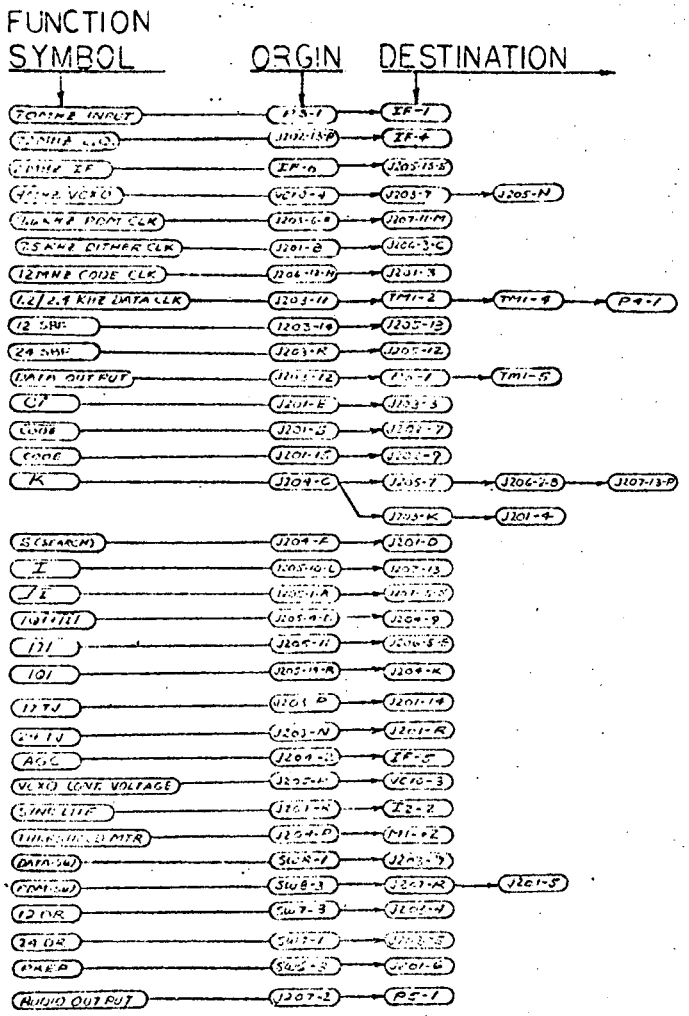


Figure 4-46. MX-291 Function Symbol Routing Diagram. (Sheet 2 of 2)

SECTION V

ALIGNMENT PROCEDURES

5.1 INTRODUCTION

The alignment procedure present here is based on back-to-back operation of two MX-290's and one MX-291. A common test setup at MRL consists of three attenuator pads, one Adams-Russell hybrid coupler, and a Boonton 91C RF voltmeter. One MX-290 is used as the interference signal and the second MX-290 is used as the desired signal to the MX-291 receiver. The power output of the MX-290 is about +6 dBm and for alignment testing the input signal into the MX-291 should be around -60 dBm to -70 dBm. By connecting a Kay attenuator to each MX-290 output and hybrid summing the two attenuator outputs, the signal plus interference signal is formed. The third attenuator input is then connected to this summed signal and its output connected to the (MX-291) receiver input. About 30 dB is set into this third attenuator pad to give isolation and insertion loss between the summer and the receiver input. The desired signal level at the hybrid summed output should be around -40 dBm, so about 45 dB attenuation is required in the signal attenuator. For a 0 dB I/S the interference signal attenuator would also have about 45 dB attenuation. To vary I/S ratios the setting of the interference attenuator pad is varied, but remember that the total power into the (MX-291) receiver should be less than -50 dBm for best performance. An acceptable test procedure is described below.

a. Check MX-290 70 MHz Carrier Oscillator

1. Remove the PDM card.
2. Connect counter to 70 MHz output BNC.
3. Set: POWER ON/OFF Switch to ON
   TX/STD-BY Switch to TX
4. Counter should read 70 MHz and if not, adjust doppler pot.

b. Check MX-290 coder clock: Connect a counter to J102 TP4 (see figure 4-7). This should read 2457300 Hz ±1 Hz. If not, adjust oscillator to 2457300 Hz.

c. Check MX-291 coder clock: Connect a counter to pin 1 of 12,286,500 Hz oscillator located on the clock board J206 (see figure 4-38). The counter should read 12286500 Hz ±1 Hz. If not, set by adjusting R16. Also, observe voltage at TP4 of J206 and if this voltage is greater than ±0.2 volt then set the voltage at TP4 equal to zero ±.05 volt dry adjusting R16. Then go to the internal frequency adjustment of the oscillator and set the oscillator to 12286500 ±1 Hz.

d. Check 72 MHz Oscillator (MX-291)

1. Set coder into NB by using NB-WB switch on coder board J201.
2. Connect the 72 MHz input signal of the 70 MHz IF can into the counter.
3. Adjust the 72 MHz oscillator to 72 MHz ±1 Hz via the adjustment located inside the 72 MHz TCXO under the screw cap.

e. Check the 4 MHz VCO: (MX-291)

1. Connect counter to J203-TP6.
2. Disconnect the 2 MHz signal jack into the 70 MHz IF can.
3. The counter should read 4 MHz ±100 Hz.
4. Adjust R105 of J205 to the required frequency.

f. Digital Receiver Board Alignment

1. Disconnect the 2 MHz output jack from the 70 MHz IF can.
2. Connect DC meter to emitter of Q3. Adjust R15 of J205 ("Q" adjustment) for zero volts.
3. Connect DC meter to emitter of "Q". Adjust R107 of J205 ("I" adjustment) for zero volts.
4. Connect DC meter to J205-11 and adjust R60 ("Q" adjustment) for zero volts.
5. Connect DC meter to J205-4, D (J205 Pin 4 of Pin D) and adjust R102 ($|I| + |Q|$ adjustment) for zero volt.
6. Connect DC meter to J205-P and adjust R105 (VCO adjustment) to zero volts.
7. Connect counter to 4 MHz VCO output at J203-TP6 (data board test point 6) and set the 4 MHz oscillator at 4 MHz ±1 Hz via the internal adjustment found under the 4 MHz crystal oscillator can screw cap.

g. MX-290 Controller Board: (Data VCO)

1. Connect scope to J203-TP5

2. Adjust R10, the blue finger adjustable pot so that a squarewave is seen at TP5. This set the data VCO on frequency, or adjusts the static phase error of the data PLL to zero.

h. MX-291 Data Board Data VCO

1. Connect scope to J203-TP4.

2. Adjust R24, the blue finger adjustable pot so that a squarewave is observed at TP4.

i. Signal AGC Adjustment

1. Connect two MX-290's via three attenuators to the MX-291; see comments in introduction).

2. Set the input signal levels to:

70 MHz signal	-60 dBm
70 MHz noise (interference)	-60 dBm

3. Set front panel controls to:

	MX-291	MX-290 (Signal)	MX-290 (Interference)
CODE SELECT	00000	00000	27777
DATA/PDM	Data	Data	Data
DATA RATE	1200	1200	1200
POWER	ON	ON	ON
PREP	Press	Press	Press
TX/STD-BY		TX	TX

Wait until sync is observed (SYNC light is on).

4. Connect scope to TEST terminal on J205 (digital receiver board).

5. This sinusoid signal should be one volt peak-to-peak ±1 volt.

6. Adjust R31 ("AGC" adjustment) pot on J204 (see 4-32 and 4-43) for one volt peak-to-peak signal.

j. I&D Filter Dump Phasing Adjustment

1. Repeat step i above.

2. Connect scope to J203-TP2.

3. Do one of the following:

(a) Connect data to DATA INPUT BNC of MX-290 signal source (Data stream must have "1's" and "0's").

(b) Connect DATA INPUT to +5 volts.

(c) Connect J103-TP1 to +5 volts.

4. Adjust "DATA VCO ADJ", see figure 4-43, so that the dump occurs at the end of each data bit.

k. H, J, Schmitt Adjustment

1. Remove J201 coder board and tape of pin D so that S cannot gate control the search drop-a-bit oscillator, and then put it back into the connector.

2. Set the input signal levels to:

70 MHz signal	None
70 MHz noise (interference)	-55 dBm

3. Set front panel controls to:

SW	MX-291	MX-290
CODE SELECT	00000	27777
DATA/PDM	Data	Data
DATA RATE	1200	1200
POWER	ON	ON
PREP	Push	Push
TX/STD-BY		TX

4. Note: THRESHOLD meter will first deflect to 7 or 8, then return to 5 or 6 after AGC noise has taken over.

5. Connect counter to J201-TP9 (see figure 4-43).

6. Adjust R6, drop-a-bit oscillator control, until the counter reads 7500 Hz.

7. Remove tape from J201-D.

8. Connect scope probe to H signal J204-TP2. (See figure 4-43).

9. Adjust R19, "H ADJ", so that this binary signal is 30% at logic zero.

10. Connect scope probe to J204-TP4.

11. Adjust R43, the "J ADJ" so that this signal is 10% at logic zero.

l. Adjust |I| + |Q| Signal

1. After completing step k-11 above, connect scope probe to J204-TP1.

2. Adjust R5 "|I| - |Q| ADJ", so that the DC voltage is at zero. See figure 4-42 where this pot is also marked |I| - |Q|.

m. Dither or Jitter Circuit Alignment

1. Set the input signal levels to: 70 MHz signal -70 dBm
70 MHz noise -80 dBm

2. Set Front Panel Controls to:

	MX-291	MX-290 Signal	MX-290 Noise
CODE SELECT	00000	00000	27777
DATA/PDM	Data	Data	Data
DATA RATE	1200	1200	1200
POWER	ON	ON	ON
PREP	Press	Press	Press
TX/STD-BY		TX	TX

3. After sync is observed, SYNC light is on.

4. Connect counter to J201-TP8.

5. Counter should read 8 kHz ±400 Hz.

6. Adjust R "dither" for about 7900 Hz on counter.

7. Increase MX-290 noise source to -50 dBm.

8. Adjust R dither and R "1.2 kHz ADJ" for minimum reading on THRESHOLD meter.

9. Set MX-290 noise to -53 dBm.

10. Set data rate switches to 2400.

11. Adjust 2400 ADJ for minimum reading on THRESHOLD meter.

12. Set MX-290 noise source to -65 dBm.

13. Adjust 9600 AZ ADJ for minimum reading on threshold meter.

SECTION VI

DRAWINGS

6.1 GENERAL

Drawings required for maintenance and troubleshooting are included in this section. Note that some of the drawings listed on the drawing list for the MX-290 and MX-291 are not included because they pertain to manufacturing. In addition, some drawings are used in support of the text.

SECTION VII

RECOMMENDATIONS

The MX-290/291 capabilities for evaluating TDRS Communications will be enhanced by incorporating any of the following equipment modifications or additions:

- Range and range rate
- Forward error control
- Narrowband DSK mode
- Wideband FSK mode
- Doppler simulation on envelope (MX-290)
- Extend performance in high RFI invironment (MX-291)
- Reduction in acquisition time
- Doppler frequency detection for acquisition and tracking (MX-291)

UFN 58

DRAWING LIST

	SPECIFICATION	TYPE — MODEL DESIGNATION	DL
GOVT.	NASA	MX-290	COMPILED BY G. Gillum DATE 6/30/71
CON-TRACTOR	MAGNAVOX		APPROVED BY M. Lorang DATE 10/7/71

ITEM NOMENCLATURE TRANSMITTER

CONTRACT NO. NAS5-16955 | DESIGN ACTIVITY: MAGNAVOX | CODE

DWG. SIZE	PART OR IDENT. NO.	REV.	CODE	NOMENCLATURE	REMARKS
C	SK42-009	X1		Diagram Schematic, Multi-Mod - J101	
C	SK42-010	X1		Diagram Schematic, Coder - J102	
C	SK42-011	X1		Diagram Schematic, Controller - J103	
D	SK42-012	X1		Diagram Schematic, PDM Conditioner - J104	
A	SK42-018	X1		MX-290, Transmitter Test Points & Adj.	
C	SK42-013	X1		Diagram, Function Symbol, Location	
C	SK42-014	X1		Diagram, Function Symbol, Routing	
D	786593*	X2		Wiring Diagram, Front Panel	
D	786594*	X2		Wiring Diagram, P. C. Connectors -J101-2-3-4	
D	786597*	X2		Wiring Diagram, Power Distribution	
A	SK-42-020			Barrier Strip Connection MX-290	
C	833420*	X1		Back Panel, MX290-291	
C	833421*	X1		Front Panel, MX290	
C	159310*	X1		Layout-Engraving, Front Panel	
C	786592	X1		Diagram Layout, Top View, MX290-291	
	E-S213809*			P. W. P. Digital Receiver	
	212306*			M. P. Digital Receiver	
	ES212317*			P. W. P. 70 MHz Amp	
	212317*			M. P. 70 MHz Amp	
	ES213799*			P. W. P. Multiplier - Mod	
	213799*			M. P. Multiplier - Mod	
D	ES213798*			Printed Wiring Board, General Purpose	
	*Drawing not included in this manual				

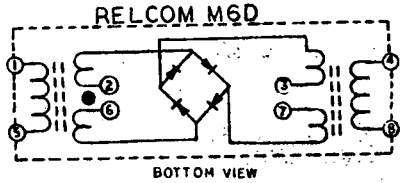
REV. SYMBOL & DATE | | | | | SHEET 1 OF 1

MRL 67797

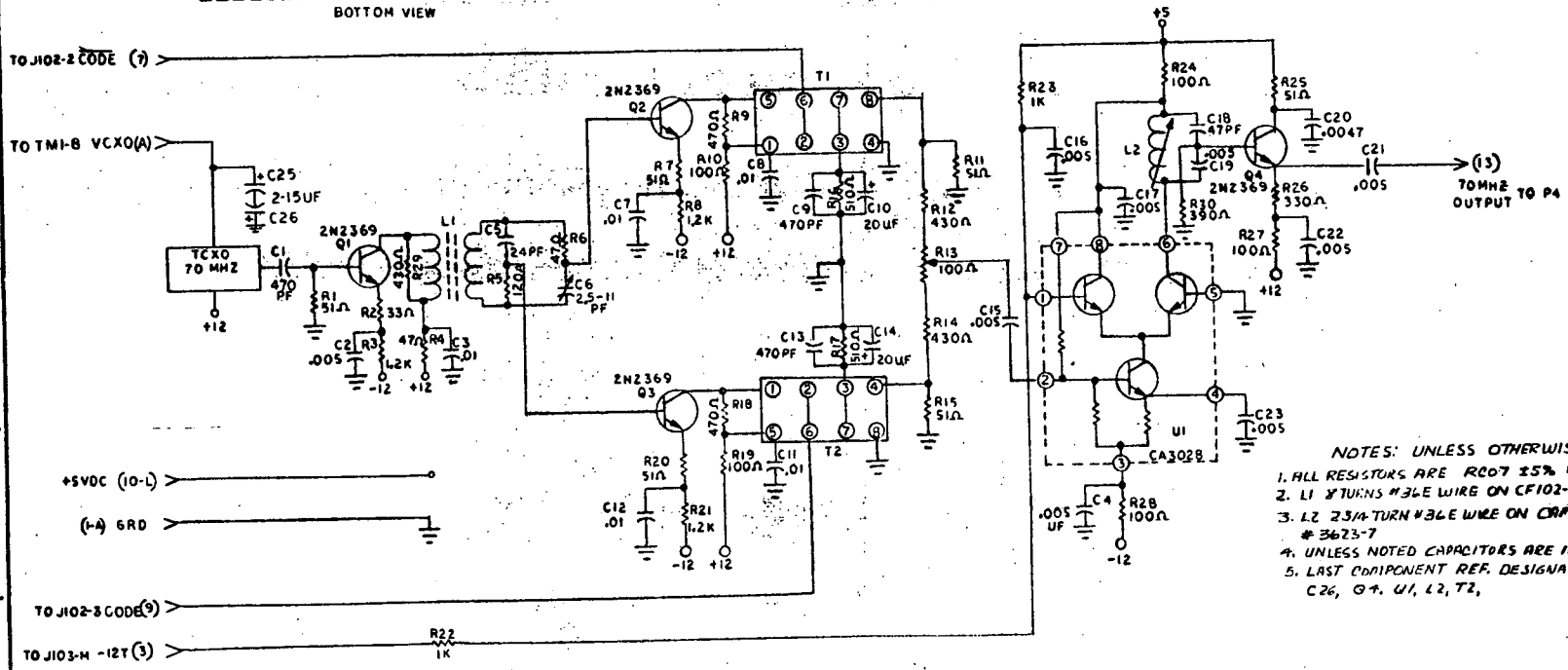
EST GROSS WT G/1000 UNITS	DWG SYSTEM NO.	-NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE J 12/1/70		

T1,2
RELCOM M6D



BOTTOM VIEW



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE RC07 ±5% 1/4 WATT.
2. L1 8 TURNS #36E WIRE ON CF102-Q3 TORROD.
3. L2 23/4 TURN #36E WIRE ON CARBIDON COIL FORM #3623-7
4. UNLESS NOTED CAPACITORS ARE IN MICROFARADS.
5. LAST COMPONENT REF. DESIGNATION USED R30 C26, Q4, U1, L2, T2,

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED
LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

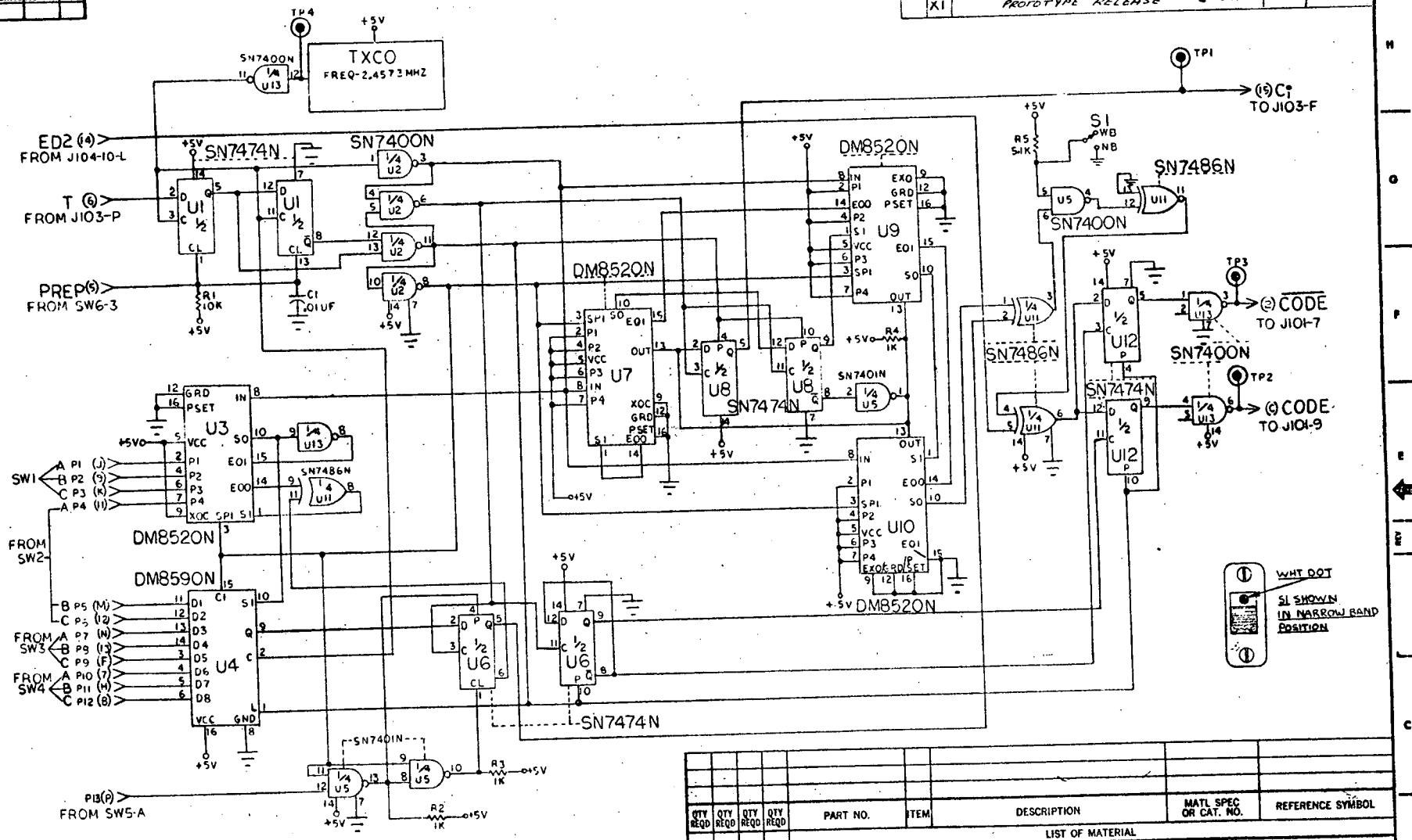
SIGNATURE	DATE
DR G. Gillum	1/1/71
CHK J. Parr	2/3/71
APP M. Lorang	2/10/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
MULTI-MOD
MX290-TRANSMITTER
J101

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-009
SCALE N/A		SHEET 1

FORM NO. 1



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE 6 9/71		

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL
						LIST OF MATERIAL		

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD
APPLICATION			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±

MATERIAL

FINISH

SIGNATURE		DATE
DR	G. Gillum	1/8/71
CHK	C. Peck	2/3/71
APP	C. Peck	2/4/71
APP	M. Lorang	2/10/71
APP		

OUTSTANDING ECN:

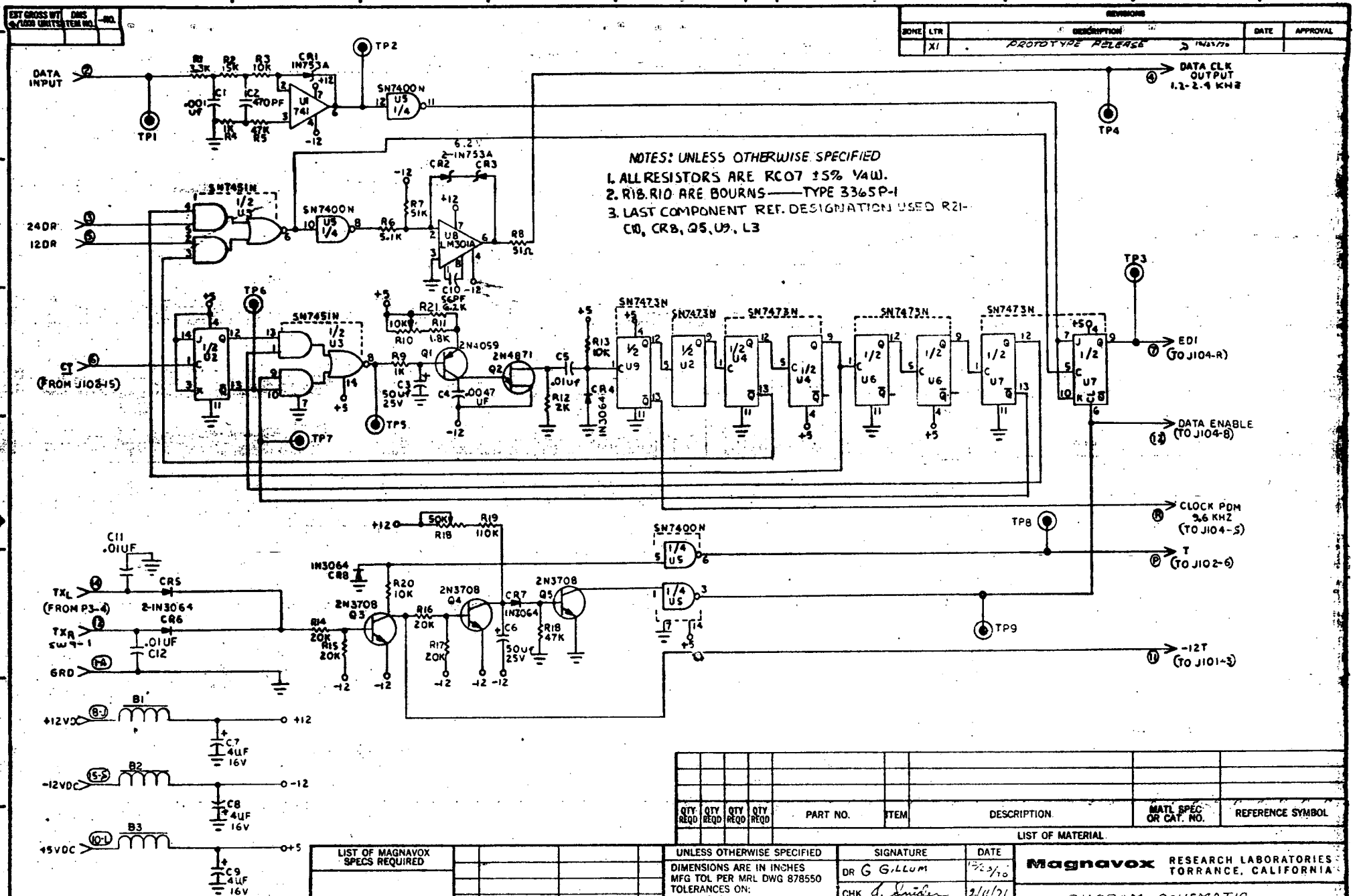
EN.

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA.

DIAGRAM- SCHEMATIC CODER MX290 TRANSMITTER J102

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-010

SCALE N/A SHEET 1 of 2



QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

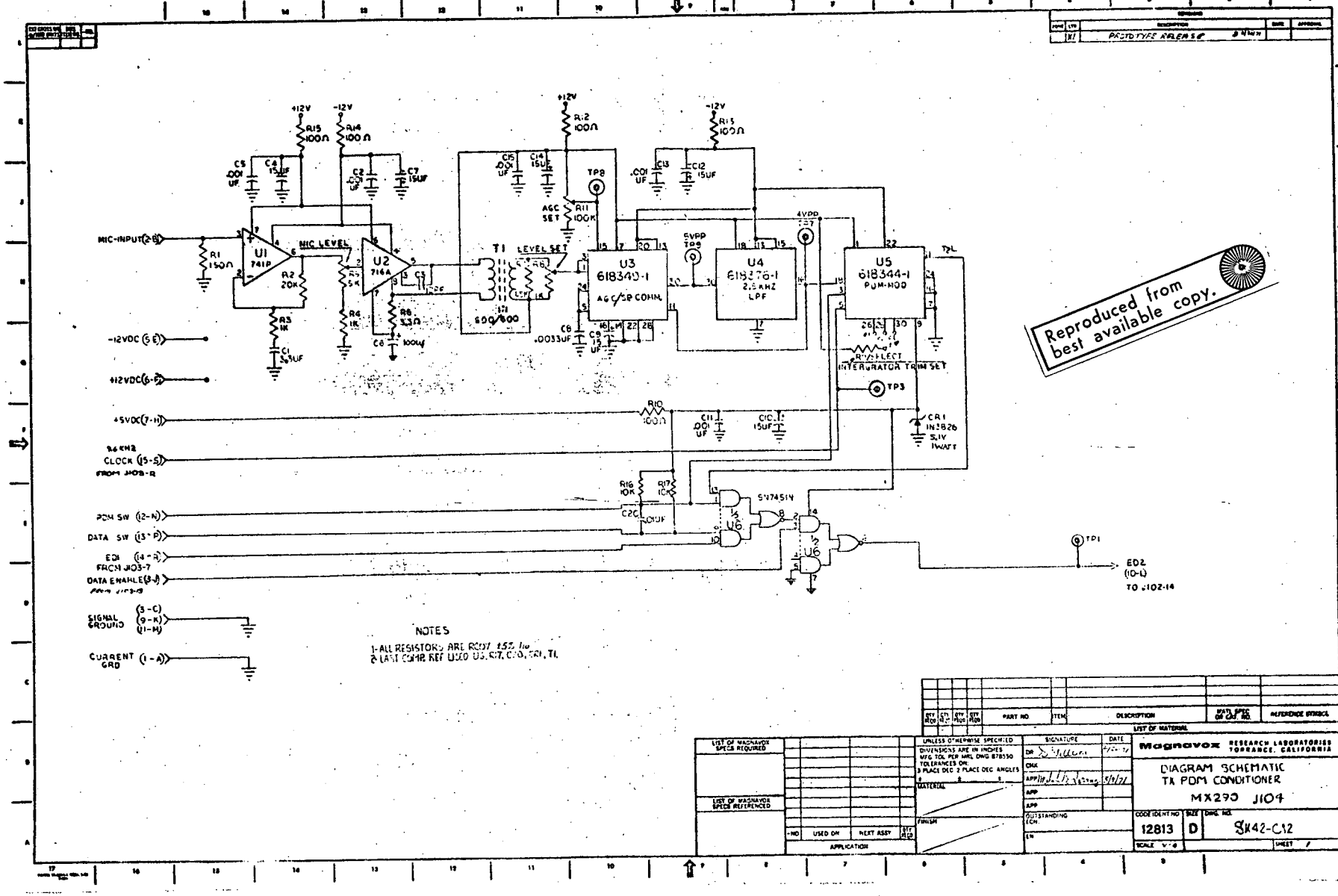
SIGNATURE	DATE
DR G GILLUM	12/23/70
CHK G. Snider	2/11/71
APP	2/11/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
CONTROLLER - TRANSMITTER
MX290
J103

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-011

SCALE N/A SHEET 1



NOTES

1- ALL RESISTORS ARE RC07 .25 W
2- LAST COMP REF USED U5, R17, C10, CR1, T1

QTY PER ASSY	QTY PER NEXT ASSY	QTY PER MAJOR	PART NO	ITEM	DESCRIPTION	MATL SPEC OR DWG NO	REFERENCE SYMBOL

LIST OF MATERIAL

-NO	USED ON	NEXT ASSY	QTY PER

APPLICATION

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG B78550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES

MATERIAL

FINISH

	SIGNATURE	DATE
DR		
CHK		
APP		5/11/71
APP		
APP		
OUTSTANDING ECN		
EN		

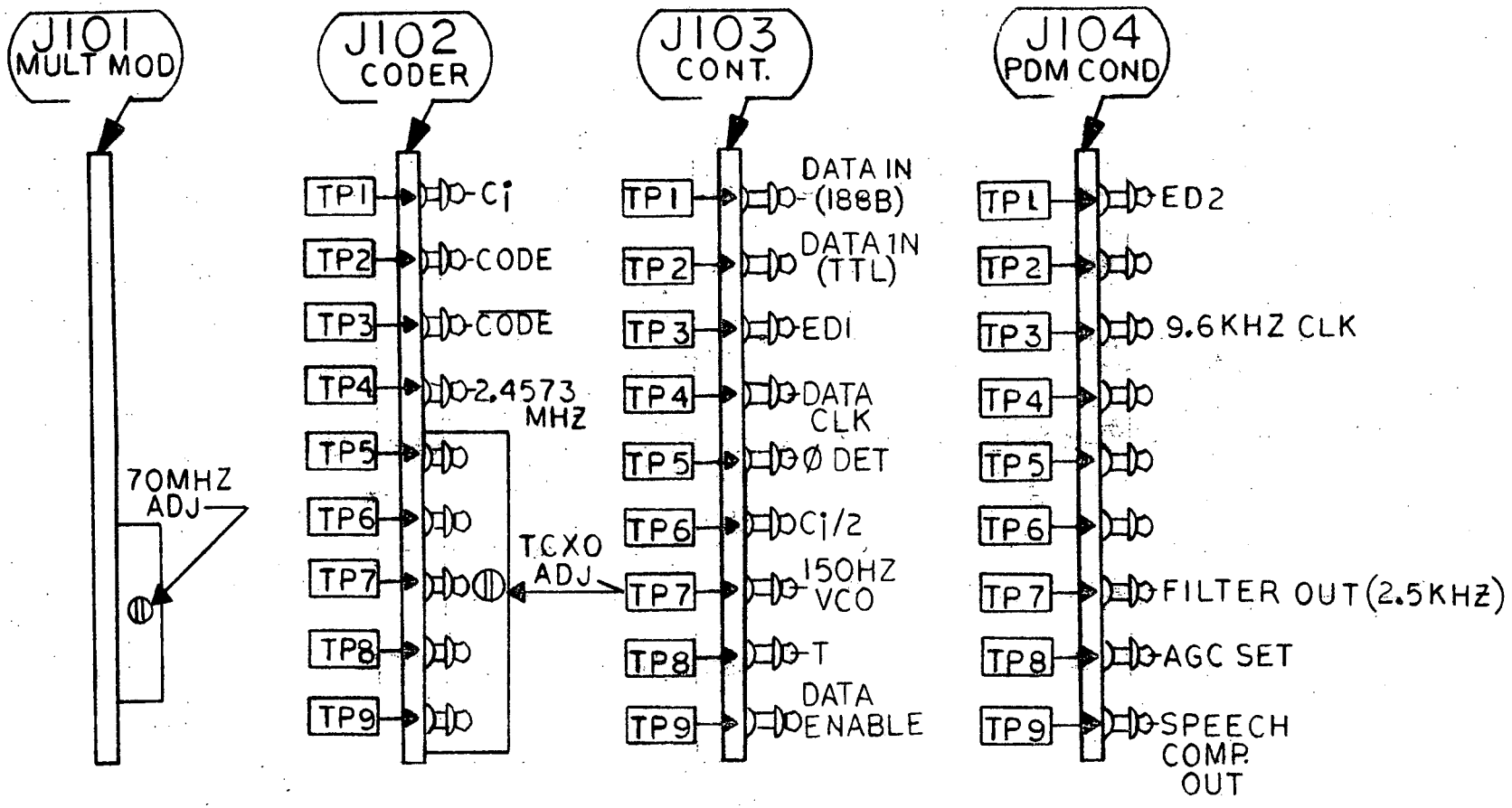
Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
TX PDM CONDITIONER
MX290 J104

CODE IDENT NO	SIZE	DWG NO
12813	D	SK42-C12

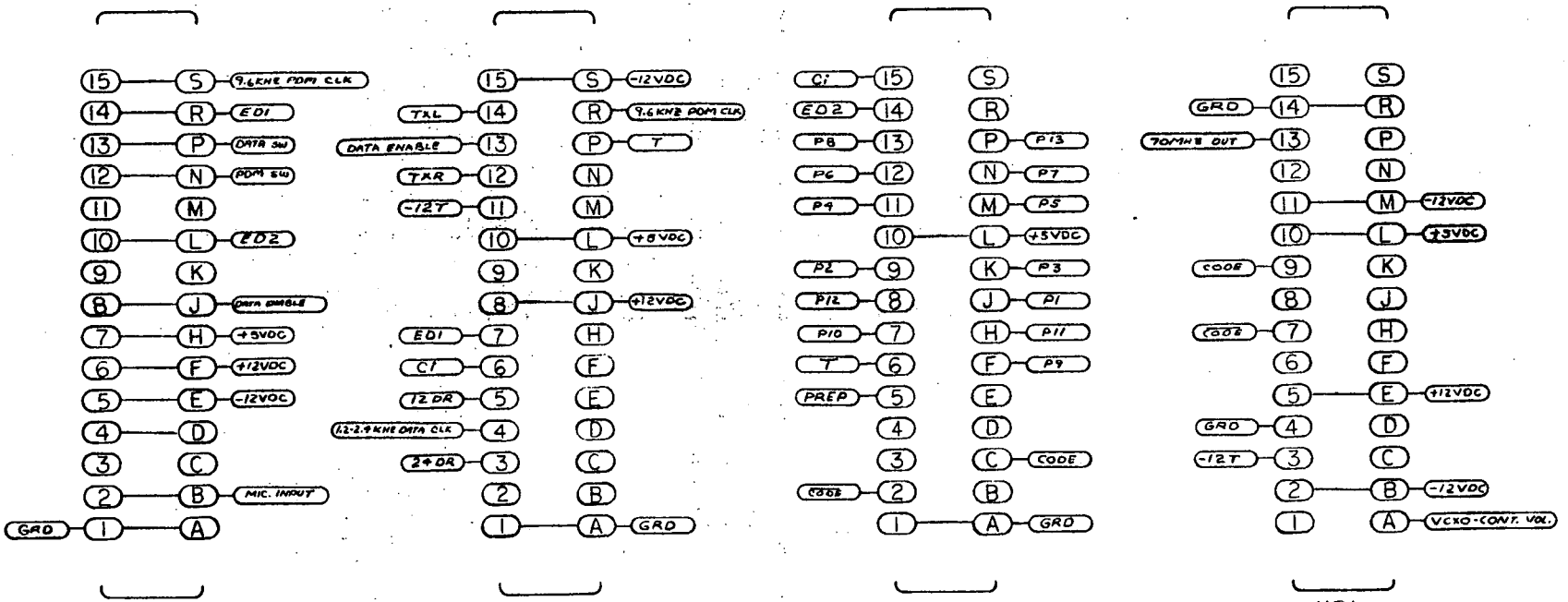
SCALE NONE SHEET 1

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED
X1	PROTOTYPE RELEASE & 6-25-71	6-25-7	M LORANG



		UNLESS OTHERWISE SPECIFIED	ORIGN G. Gillum	6-25-71	Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA
		DIMENSIONS ARE IN INCHES	CHK		
		XXX = ±.010	APVD M. LORANG	6-25-71	MX290 XMTR
		XX = ±.02	APVD		TEST POINTS & ADJ.
		ANGLE = ±0.5°	APVD		
		MATERIAL	CONTR. DEGN. APPVL.		SIZE A | CODE IDENT NO 12813 | DRAWING NO SK42-018
		FINISH	GOVT. CONTR. NO.		
NEXT ASSY	USED ON		GOVT ACTIVITY APPROVAL		SCALE N/A | DWG LEVEL | SHEET 1 OF
APPLICATION					

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE 4/23/71		



QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED
LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE	DATE
DRG. G. Ilum	4/23/71
CHK	
APP W. L. Lk. Downey	5/11/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

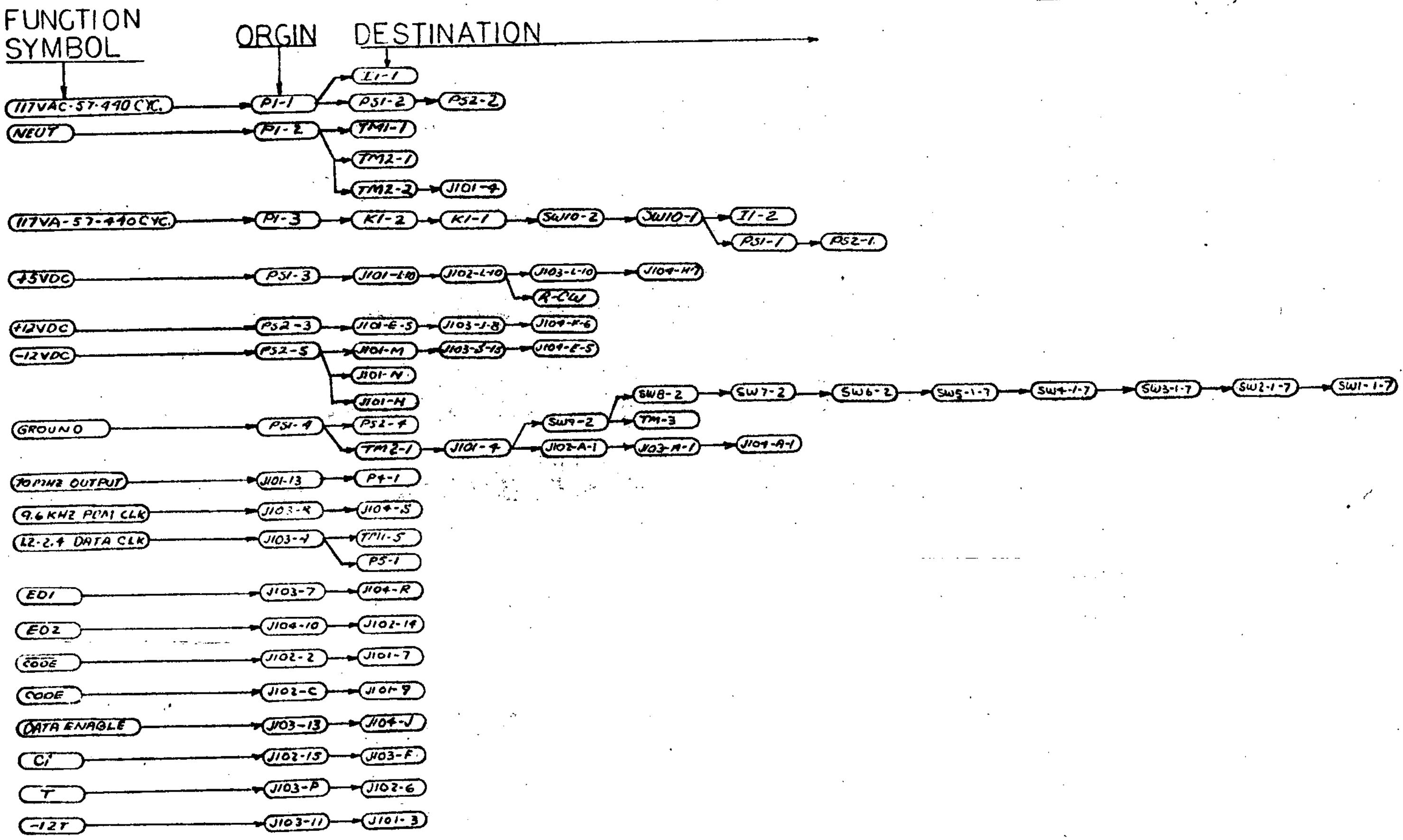
Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM FUNCTION SYMBOL LOCATION MX290

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK 42-013

SCALE N/A SHEET 1

FORM NO. 1



EST GROSS WT g/1000 UNITS	DWG ITEM NO.	-NO.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE	9/21/71	

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC ± 2 PLACE DEC ± ANGLES ±
MATERIAL
FINISH

SIGNATURE	DATE
DR G Gillum	4/27/71
CHK	
APP [signature]	5/7/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM
FUNCTION SYMBOL ROUTING
MX290

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-014
SCALE N/A		SHEET 1

FORM NO. 1

7

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

CONNECTIONS ON BARRIER STRIP MX290

*
PIN 1. SAFTY GROUND.

PIN 2. DATA IN BACK PANEL.
PIN 3. SHIELD GROUND.
PIN 4. DATA IN FRONT PANEL.

JUMPER IF FEEDING DATA FROM FRONT PANEL BNC. REMOVE IF FEEDING DATA FROM REAR PANEL THRU PIN 2.

PIN 5. DATA CLOCK OUT.

PIN 6. TXR, REMOTE TX.

PIN 7. R-S, DOPPLER CONTROL SWINGER.
PIN 8 VCO CONTROL LINE.
PIN 9 REMOTE DOPPLER INPUT BNC BACK PANEL.

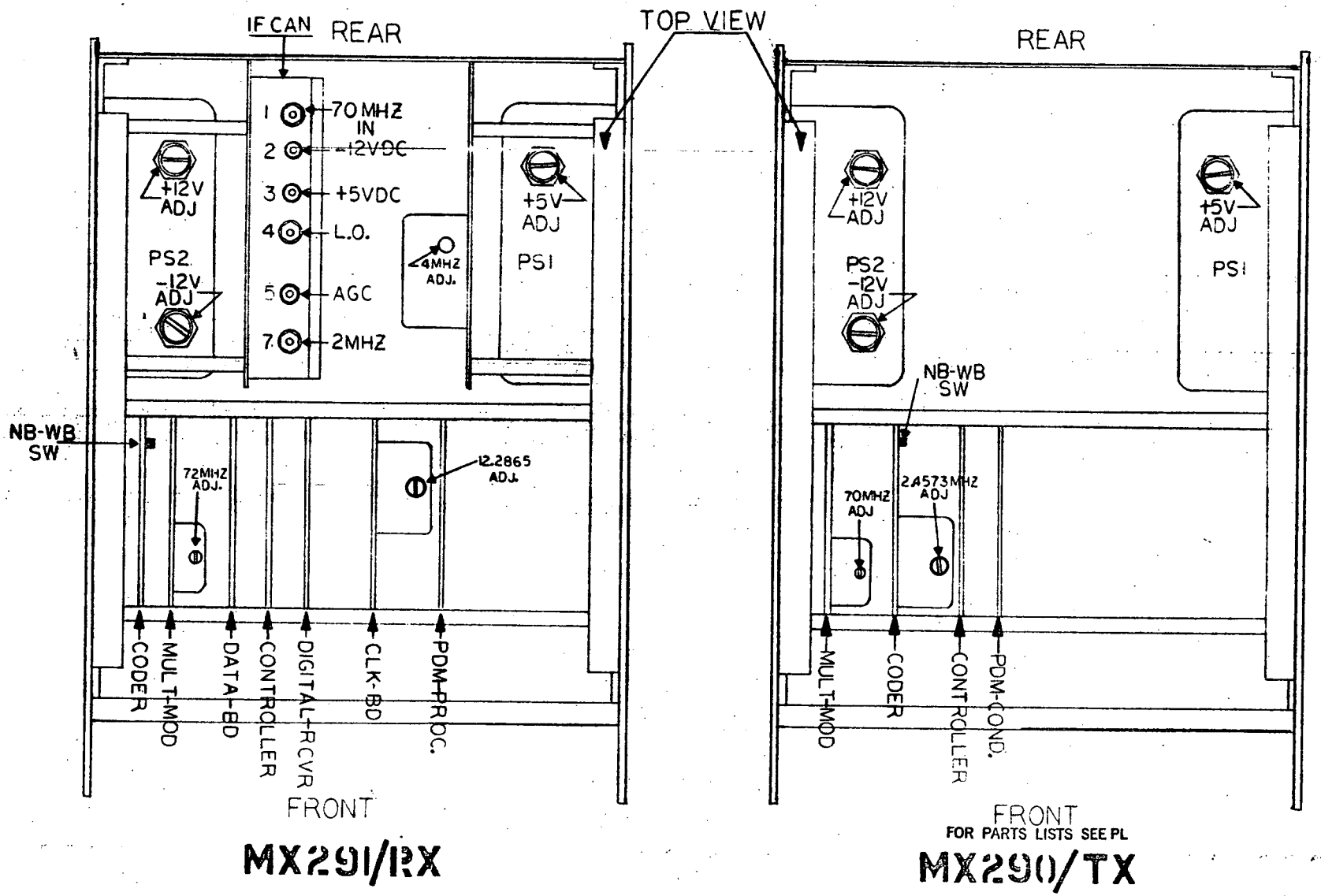
SEE NOTE

*PIN 1. LEFT SIDE WHEN FACING BACK PANEL.

NOTE:
WHEN USING DOPPLER CONTROL ON FRONT PANEL, JUMPER PIN 7 AND 8.
IF REMOTE DOPPLER IS USED JUMPER PIN 8 AND 9.

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES XXX = ±.010 XX = ±.02 ANGLE = ±0.5°	ORIGN Gillum		Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA
			CHK BYROADS		
			APVD MLorang		BARRIER STRIP CONNECTION MX290
			APVD		
		MATERIAL	APVD		
	MX290		CONTR. DEGN. APPVL.		SIZE A | CODE IDENT NO 12813 | DRAWING NO SK-92-020.
NEXT ASSY	USED ON	FINISH	GOVT. CONTR. NO.		SCALE | DWG LEVEL | SHEET 1 OF —
APPLICATION			GOVT ACTIVITY APPROVAL		

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	X1	PROTOTYPE RELEASE	6-4-71	



			UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES XXX = ±.010 XX = ±.02 ANGLE = ±0.5°	ORIGN G Grillon	6/14/71
			MATERIAL	CHK	
				APVD M. M. LORRAINE	6/14/71
				APVD	
			FINISH	APVD	
				GOVT CONTRACT NUMBER	
				CONTRACT DESIGN APPROVAL	
DASH NO	NEXT ASSY	USED ON	APPLICATION	GOVT ACTIVITY APPROVAL	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM LAYOUT
TOP VIEW
MX290/TX-MX291/RX

SIZE	CODE IDENT NO	DRAWING NO
C	12813	786592

SCALE N/A | DWG LEVEL | SHEET 1

UFN 58

DRAWING LIST

	SPECIFICATION	TYPE – MODEL DESIGNATION	DL
GOVT.	NASA	MX-291	COMPILED BY G. Gillum DATE 7/1/71
CON-TRACTOR	MAGNAVOX		APPROVED BY M. Lorang DATE 10/7/71

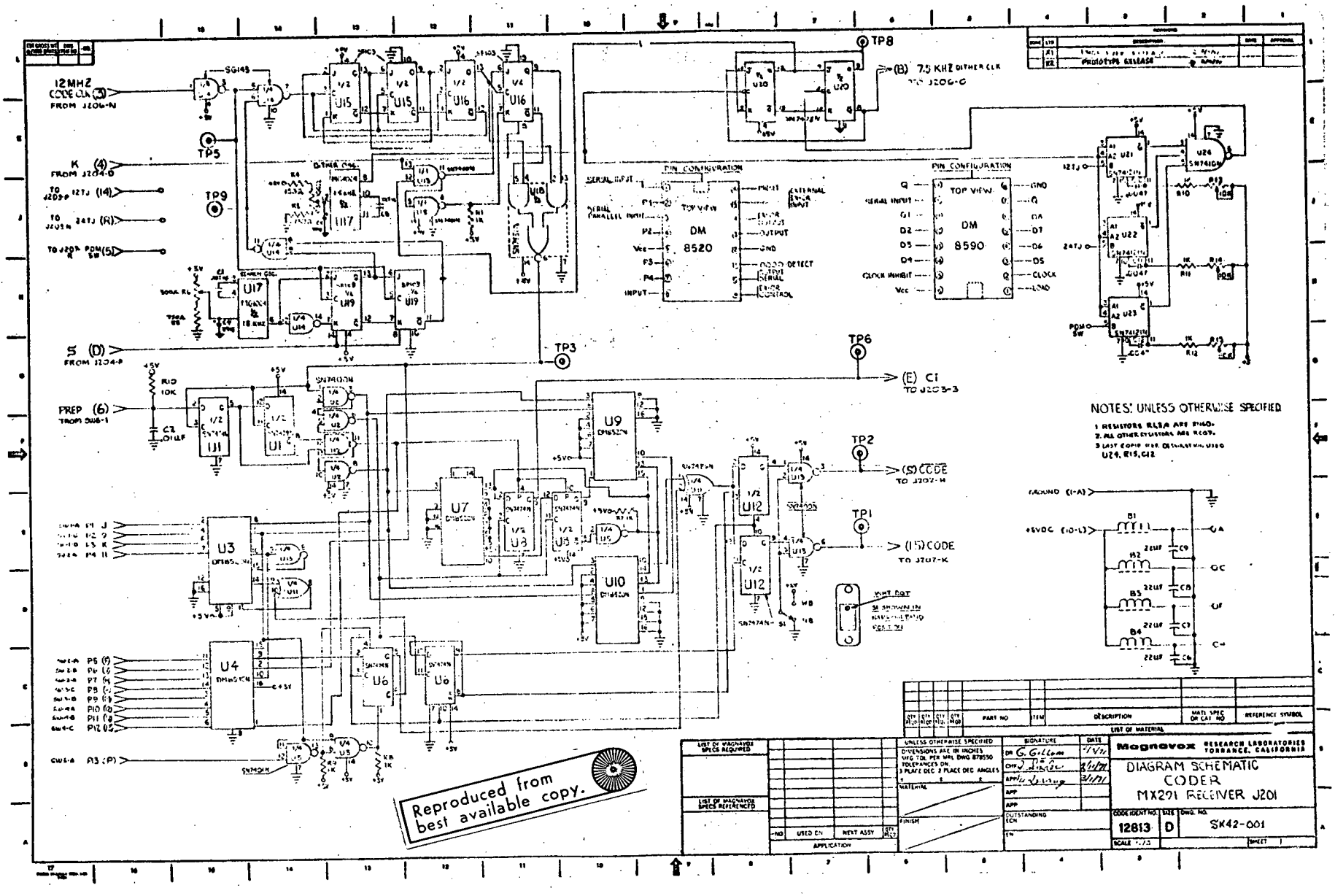
ITEM NOMENCLATURE RECEIVER

CONTRACT NO.	DESIGN ACTIVITY: MAGNAVOX, URBANA, ILLINOIS	CODE

DWG. SIZE	PART OR IDENT. NO.	REV.	CODE	NOMENCLATURE	REMARKS
D	SK41-001	X2		Diagram Schematic, Coder - 3201	
C	Sk42-002	X1		Diagram Schematic Multi-Mod - J202	
C	SK42-003	X2		Diagram Schematic Data Board - J203	
D	SK42-004	X1		Diagram Schematic Receiver Controler - J204	
E	SK42-005	X1		Diagram Schematic Digital Receiver - J205	
C	SK42-006	X2		Diagram Schematic Clock Board - J206	
C	SK42-007	X1		Diagram Schematic Receiver Processor - J207	
D	SK42-008	X1		Diagram Schematic, 70 MHz Amp.	
C	SK42-015	X1		Diagram, Function Symbol Routing	2 Sheets
C	SK42-016	X2		Diagram, Function Symbol Location	
B	SK42-017	X1		MX-291 Receiver, Test Points and Adj.	
A	SK42-021	X1		Barrier Strip Connections - MX-291	
D	786595*	X2		Wiring Diagram, P.C. Connectors	
D	786596*	X2		Wiring Diagram, Front, Rear Panels, and Power Distribution	
C	833422*	X1		Front Panel	
C	833420*	X1		Back Panel, MX290-291	
C	159311*	X1		Layout Engraving, Front Panel	
A	SK42-022	X1		Diagram Schematic Speaker Amplifier	
	* Drawing not included in this manual				

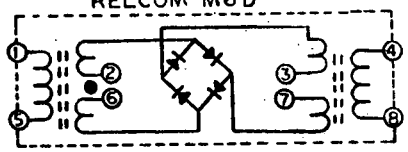
REV. SYMBOL & DATE					SHEET 1 OF

MRL 67797

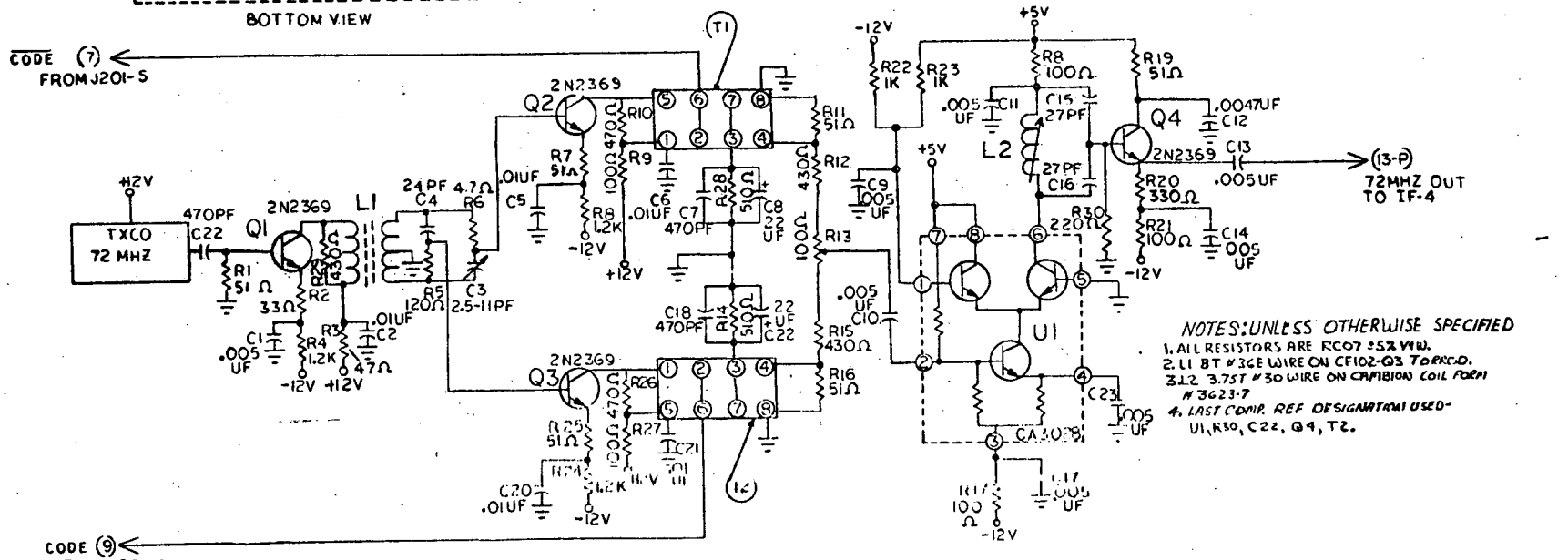

12MHZ CODE CLK (3) FROM J206-N
K (4) FROM J204-G
TO J209-P 12TJ (14)
TO J203-N 24TJ (R)
TO J204-P PDM(5)
S (D) FROM J204-P
PREP (6) FROM J206-1
TP5
TP9
TP3
TP8
TP6
TP2
TP1
(B) 7.5 KHZ DITHER CLK TO J206-G
(E) CI TO J203-3
(S) CODE TO J207-H
(15) CODE TO J207-K
PIN CONFIGURATION
DM 8520
DM 8590
NOTES: UNLESS OTHERWISE SPECIFIED
1 RESISTORS R1,2,A ARE 1%Ω.
2. ALL OTHER RESISTORS ARE ±10%.
3 LAST COMP. USED.
U29, R15, C12
GROUND (1-A)
+5VDC (10-L)
Reproduced from best available copy.
Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA
DIAGRAM SCHEMATIC
CODER
MX291 RECEIVER J201
12813
D
SK42-001

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE	2/1/71	

T1-2
RELCOM M6D



BOTTOM VIEW



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE RC07 ±5% WW.
2. L1 BT #36E WIRE ON CF102-Q3 TORCOID.
3. L2 3.75T #30 WIRE ON CAMBION COIL FORM #3623-7
4. LAST COMP. REF DESIGNATION USED- U1, R30, C22, Q4, T2.

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED					
LIST OF MAGNAVOX SPECS REFERENCED					
	-NO.	USED ON	NEXT ASSY	QTY REQD	
	APPLICATION				

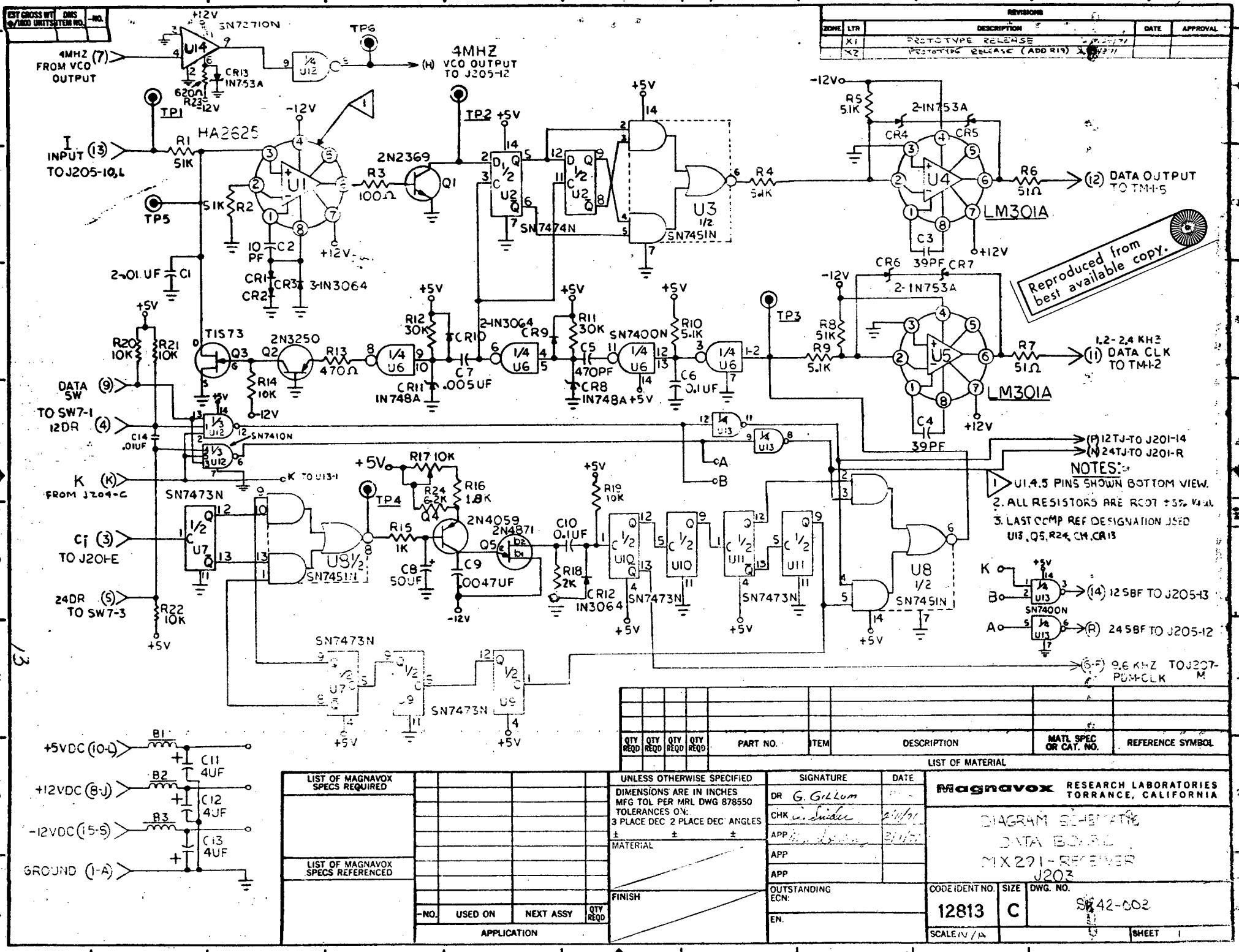
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE		DATE
DR	G Gillum	2/1/71
CHK	C. Page	2/3/71
APP	M. Doran	2/8/71
APP		
APP		
OUTSTANDING ECN:		
EN.		

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
MULTI-MOD
MX291 RECEIVER
J202

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-002
SCALE N/A		SHEET 1



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE		
	X2	PROTOTYPE RELEASE (ADD R19)		

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED				
LIST OF MAGNAVOX SPECS REFERENCED				
-NO.	USED ON	NEXT ASSY	QTY REQD	
APPLICATION				

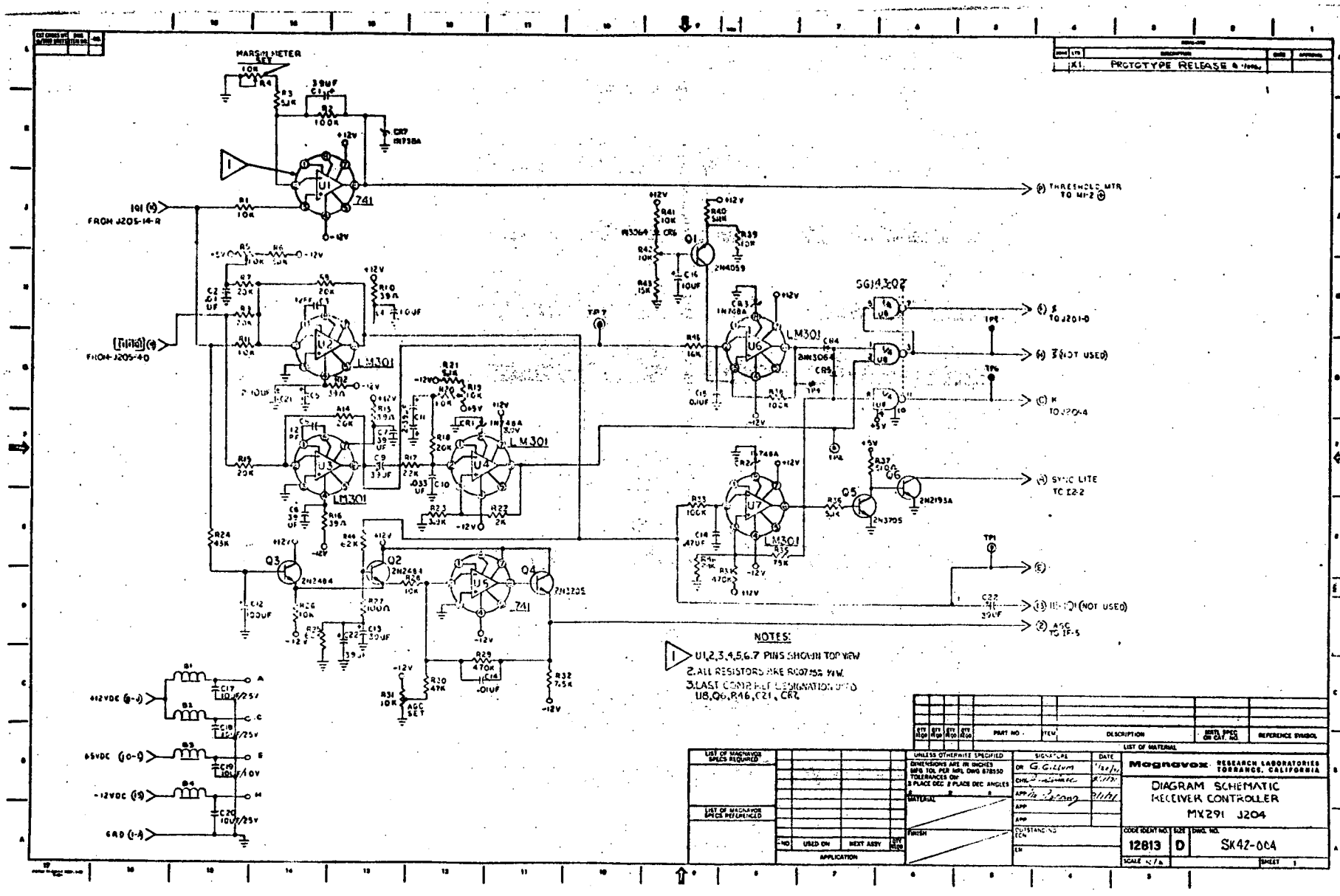
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

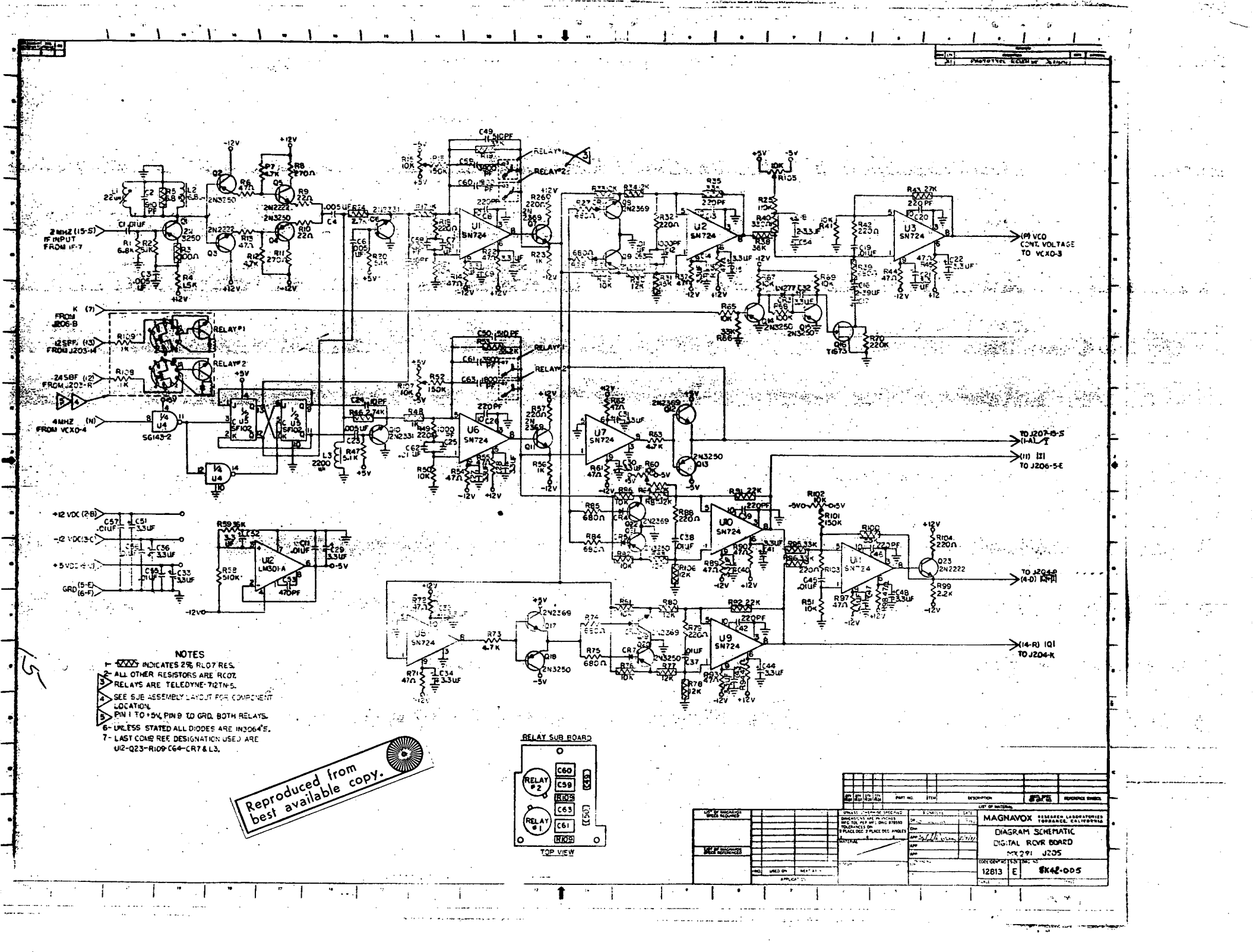
SIGNATURE		DATE
DR	G. Gillum	
CHK		
APP		
APP		
APP		
OUTSTANDING ECN:		
EN.		

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
DATA BOARD
MX221-RECEIVER
J202

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	S842-002
SCALE N/A		SHEET 1

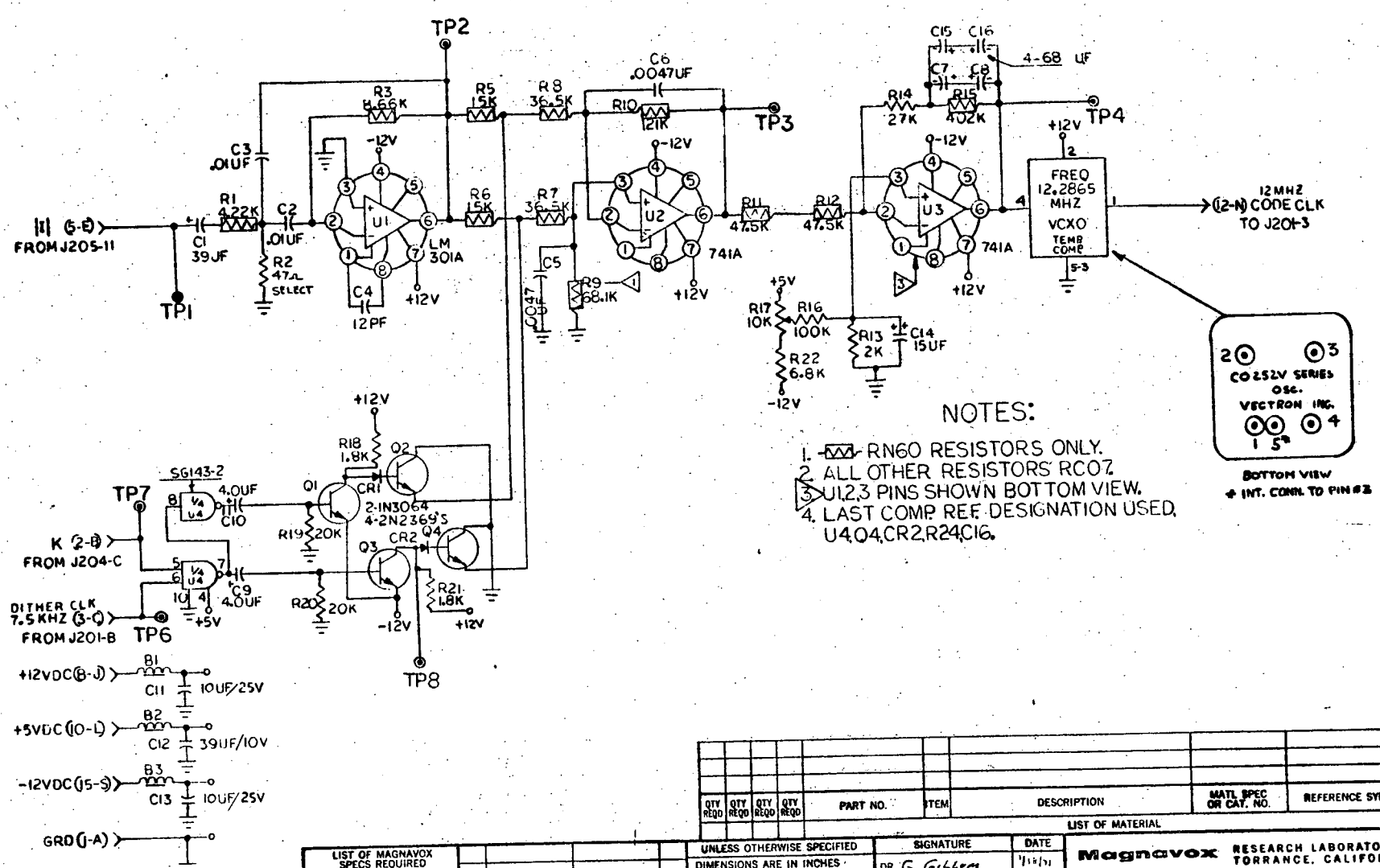

MARSH METER SET
741
LM301
2N4059
2N2484
2N3705
2N2193A
SG1430?
NOTES:
1. U1,2,3,4,5,6,7 PINS SHOWN TOP VIEW
2. ALL RESISTORS ARE RC07GF PKW.
3. LAST COMPONENT DESIGNATION USED U8, Q6, R46, C21, CR7.
PROTOTYPE RELEASE
DIAGRAM SCHEMATIC
RECEIVER CONTROLLER
MX291 J204
Magnavox
RESEARCH LABORATORIES TORRANCE, CALIFORNIA
12813
D
SK42-004



NOTES

1- XXXX INDICATES 2% RL07 RES.
2- ALL OTHER RESISTORS ARE RC07.
3- RELAYS ARE TELEDYNE-712TN-5.
4- SEE SUB ASSEMBLY LAYOUT FOR COMPONENT LOCATION.
5- PIN 1 TO +5V, PIN 9 TO GRD. BOTH RELAYS.
6- UNLESS STATED ALL DIODES ARE IN3064'S.
7- LAST COMP. REF. DESIGNATION USED ARE U12-Q23-R109-C64-CR7 & L3.

MAGNAVOX RESEARCH LABORATORIES TORRANCE, CALIFORNIA		
DIAGRAM SCHEMATIC DIGITAL RCVR BOARD MX291 J205		
12813	E	8K42-005



NOTES:

1. RN60 RESISTORS ONLY.
2. ALL OTHER RESISTORS RC07.
3. U1,2,3 PINS SHOWN BOTTOM VIEW.
4. LAST COMP. REF. DESIGNATION USED. U4,Q4,CR2,R24,C16.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	1X1	PROTOTYPE RELEASE	2/11/71	
	1X2	R19-R17 DELETED	3/31/71	

LIST OF MATERIAL

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE		DATE
DR	G. Gillom	2/11/71
CHK	J. Snider	2/11/71
APP	Mr. Lorang	3/17/71
APP		
APP		

OUTSTANDING ECN:
EN.

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
CLOCK BOARD
MX 291-RCVR-J206

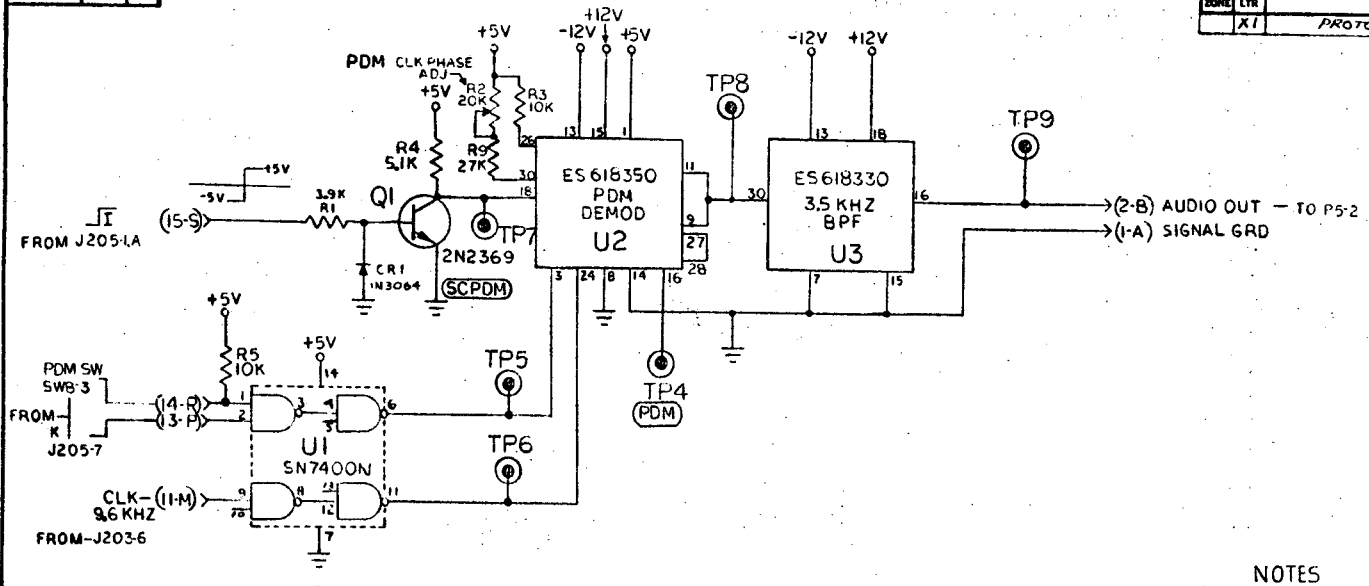
CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-006

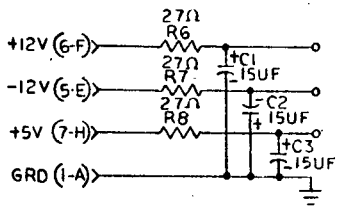
SCALE N/A SHEET 1

FORM NO. 1

EST GROSS WT #/1000 UNITS	DMS SYSTEM NO.	NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE REL. 9-20-71		





NOTES
1-UNLESS STATED ALL RESISTORS ARE RC07 5% ¼W.
2. LAST COMP. REF. DESIGNATIONS- U3, Q1, R9, C3.

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED
LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE	DATE
DR G Gillum	5/13/71
CHK	
APP Richard M Bovang	5/1/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

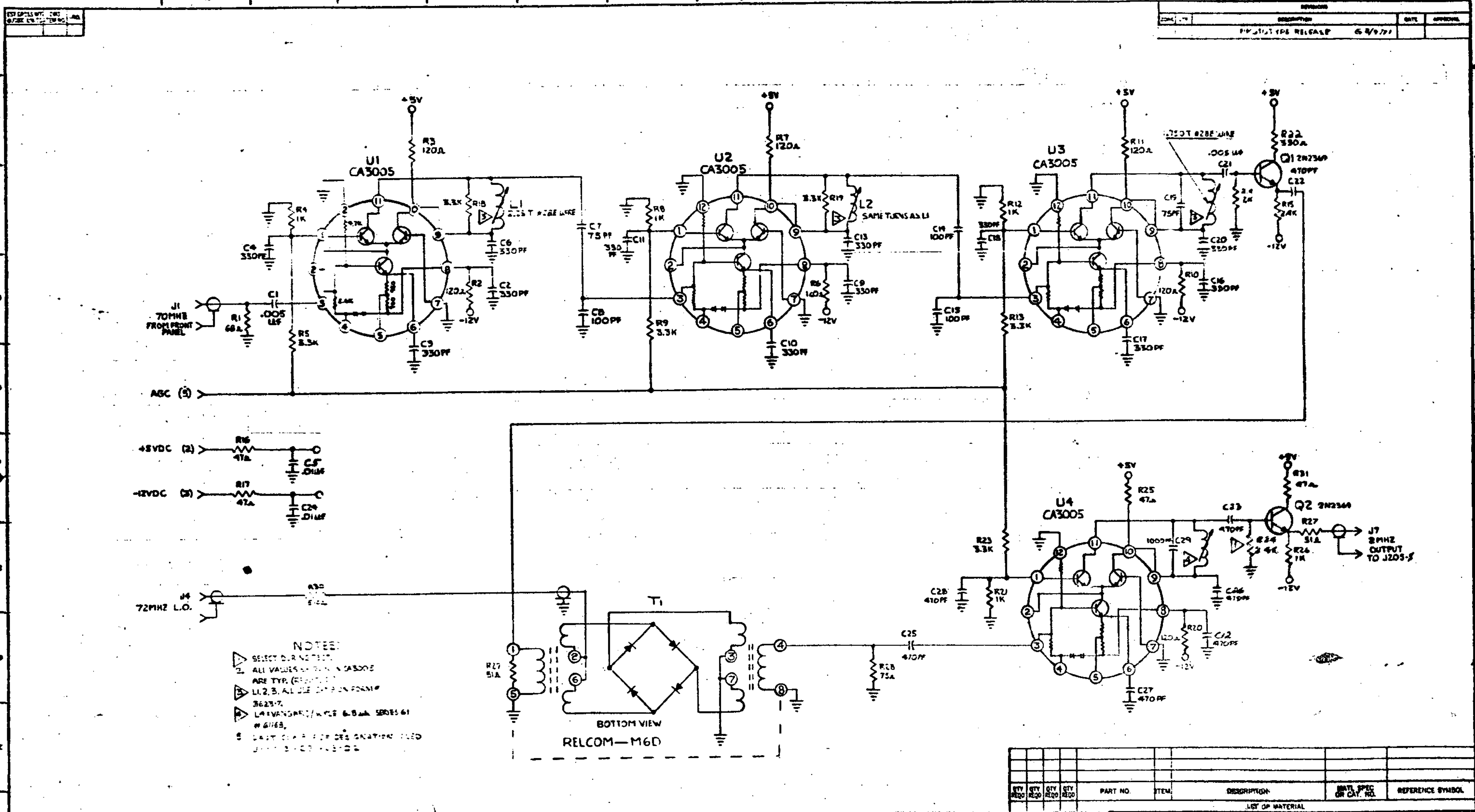
Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
RECEIVER PDM PROCESSOR
MX291
J207

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	8142-007

SCALE N/A SHEET 1

PDRM NO. 1



LIST OF MAGNAVOX SPECS REQUIRED
LIST OF MAGNAVOX SPECS REFERENCED

UNLESS OTHERWISE SPECIFIED	SIGNATURE	DATE
DIMENSIONS ARE IN INCHES MFG TOL PER MRL DWG 878550 TOLERANCES ON: 3 PLACE DEC 2 PLACE DEC ANGLES	DR G. Gillum	5/9/71
MATERIAL	CHK	
FINISH	APP	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC 70 MHZ AMP MX291 RCVR

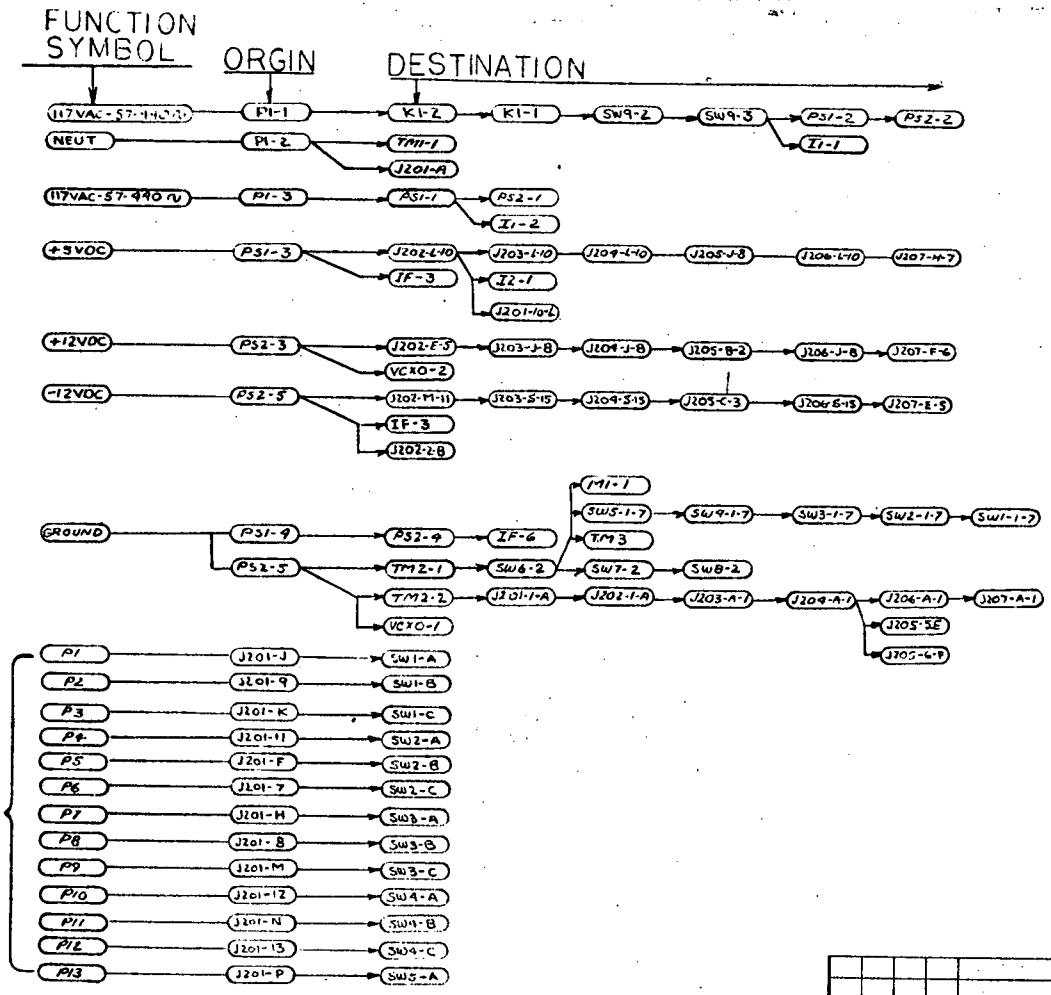
CODE IDENT NO	SIZE	DWG. NO.
12813	D	SK 42-008

SCALE N/A SHEET 1

18

LST GROSS WT #/1000 UNITS	DWG SYSTEM NO.	ITEM NO.	NO

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
		PROTOTYPE RELEASE 3 9h3/71		



CODE SELECT

P1	J201-J	SW1-A
P2	J201-9	SW1-B
P3	J201-K	SW1-C
P4	J201-11	SW2-A
P5	J201-F	SW2-B
P6	J201-7	SW2-C
P7	J201-H	SW3-A
P8	J201-8	SW3-B
P9	J201-M	SW3-C
P10	J201-12	SW4-A
P11	J201-N	SW4-B
P12	J201-13	SW4-C
P13	J201-P	SW5-A

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED	LIST OF MAGNAVOX SPECS REFERENCED

-NO.	USED ON	NEXT ASSY	QTY REQD
APPLICATION			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE		DATE
DR	G. Gillum	9/23/71
CHK		
APP	[illegible]	5/7/71
APP		
APP		
OUTSTANDING ECN:		
EN.		

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM
FUNCTION SYMBOL ROUTING
MX291

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-015
SCALE n/a		SHEET 1 OF 2

61

EST GROSS WT.	DWG SIZE	NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE	4/16/71	

FUNCTION SYMBOL ROUTING

FUNCTION SYMBOL	ORGIN	DESTINATION		
70MHz INPUT	J1[illegible]-1	IF-1		
72MHz L.O.	J102-13-P	IF-4		
2MHz IF	IF-6	J205-15-S		
4MHz VCXO	VCXO-4	J203-7	J205-N	
9.6KHz PDM CLK	J203-6-F	J207-11-M		
7.5 KHz DITHER CLK	J201-B	J206-3-C		
12MHz CODE CLK	J206-12-N	J201-3		
1.2/2.4 KHz DATA CLK	J203-11	TM1-2	TM1-4	P4-1
12 SBF	J203-14	J205-13		
24 SBF	J203-R	J205-12		
DATA OUTPUT	J[illegible]-12	TM1-1	TM1-5	
C1	J201-E	J203-3		
CODE	J201-5	J202-7		
CODE	J201-15	J202-9		
K	J204-C	J205-1	J206-2-B	J207-13-P
		J203-K	J201-4	
E (SEARCH)	J204-E	J201-D		
I	J205-10-L	J203-13		
/I/	J205-1-A	J201-15-R		
|Q+I|	J205-4-D	J204-9		
|I|	J205-11	J204-5-E		
|Q|	J205-14-R	J204-K		
12 TJ	J203-P	J201-14		
24 TJ	J203-N	J201-R		
AGC	J204-3	IF-5		
VCXO CONT. VOLTAGE	J205-P	VCXO-3		
SYNC LITE	J201-N	I2-2		
THRESHOLD MTR	J204-P	TM1-[illegible]		
DATA SW	SW8-1	J203-7		
PDM SW	SW8-3	J207-R	J201-5	
12 DR	SW7-3	J205-9		
24 DR	SW7-1	J[illegible]-5		
PREP	SW[illegible]-2	J201-6		
AUDIO OUTPUT	J207-2	P5-1		

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED	NO.	USED ON	NEXT ASSY	QTY REQD
LIST OF MAGNAVOX SPECS REFERENCED		APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE	DATE
DR G. Gilliam	4/14/71
CHK	
APP [illegible]	5/26/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

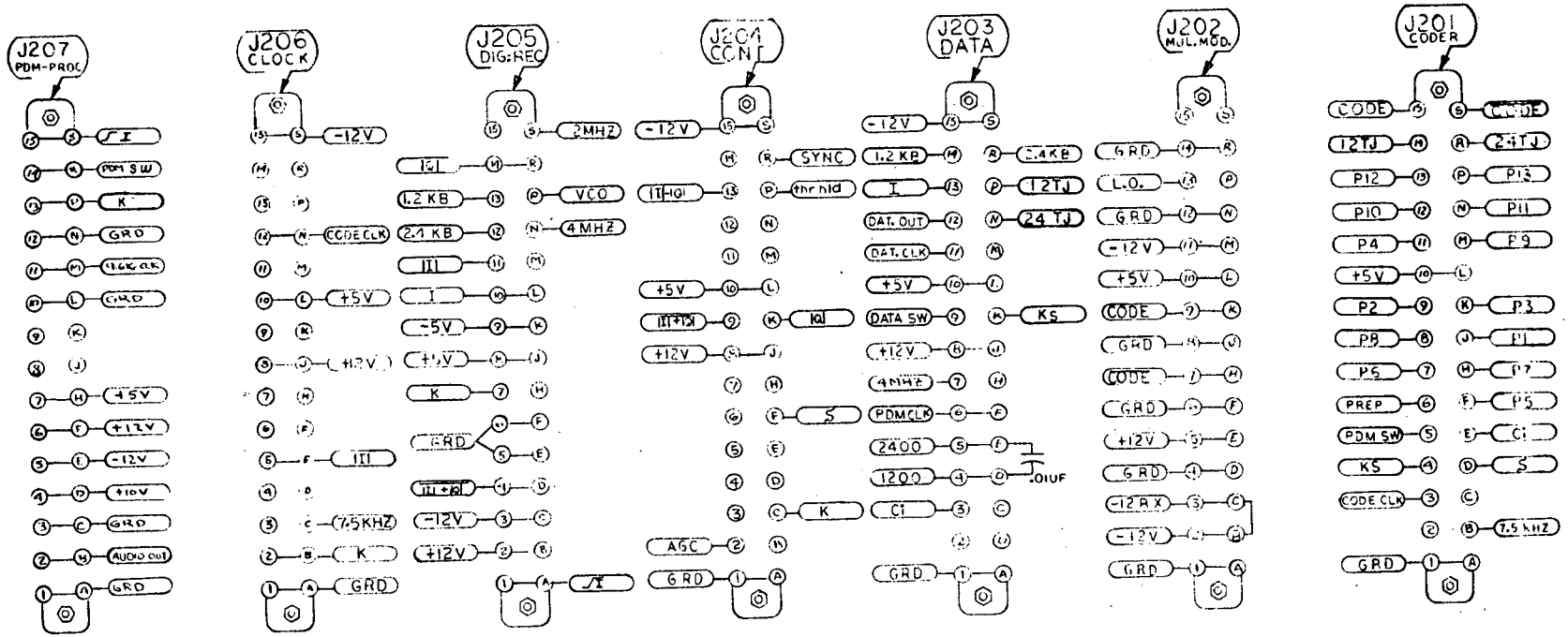
Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM
FUNCTION SYMBOL ROUTING
MX291

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SY42-215
SCALE: V/4		SHEET 2

FORM NO. 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE	2/28/71	
	X2	PROTOTYPE RELEASE (ADD -01 J203-9-5)	3/11/71	



QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT. NO.	REFERENCE SYMBOL

LIST OF MATERIAL

LIST OF MAGNAVOX SPECS REQUIRED	-NO.	USED ON	NEXT ASSY	QTY REQD
		MX291		
LIST OF MAGNAVOX SPECS REFERENCED	APPLICATION			

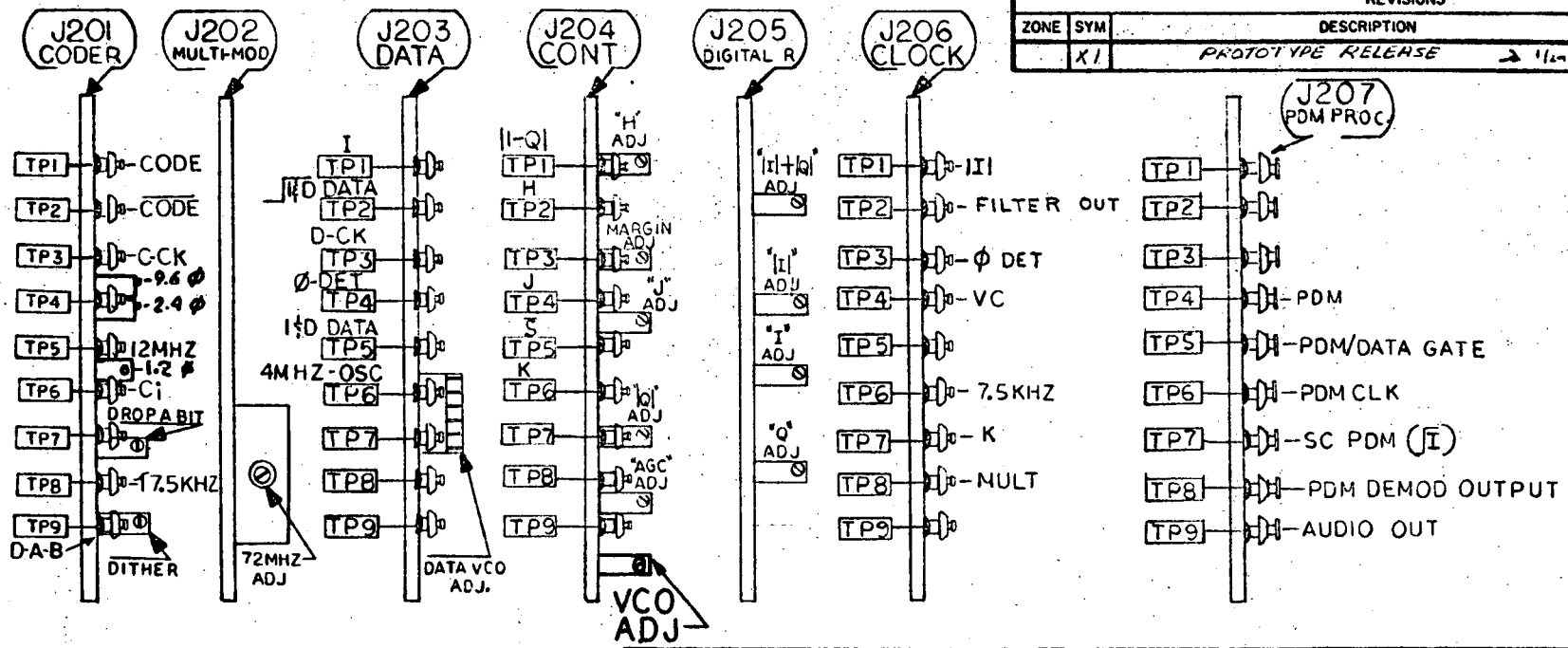
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC 2 PLACE DEC ANGLES
± ± ±
MATERIAL
FINISH

SIGNATURE	DATE
DR G. Gillum	2/2/71
CHK D. Smith	2/11/71
APP	3/1/71
APP	
APP	
OUTSTANDING ECN:	
EN.	

Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA

DIAGRAM
FUNCTION SYMBOL LOCATION
MX291 RECEIVER

CODE IDENT NO.	SIZE	DWG. NO.
12813	C	SK42-016
SCALE		SHEET



REVISIONS

ZONE	SYM	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE → 1/29/71		

REV

QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART NO.	ITEM	DESCRIPTION	MATL SPEC OR CAT NO.	REFERENCE SYMBOL

LIST OF MATERIAL

REV

-NO.	USED ON	NEXT ASSY	QTY REQD
	MX291		

APPLICATION

LIST OF MAGNAVOX SPECS REQUIRED

LIST OF MAGNAVOX SPECS REFERENCED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
MFG TOL PER MRL DWG 878550
TOLERANCES ON:
3 PLACE DEC ± 2 PLACE DEC ± ANGLES ±

MATERIAL

FINISH

SIGNATURE	DATE
DR G. GILLUM	1/29/71
CHK	
APP	
APP	
APP	

OUTSTANDING ECN:

EN:

Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

MX291 RECEIVER
TEST POINTS AND ADJ.

CODE IDENT NO.	SIZE	DWG NO.
12813	B	5142-017

SCALE N/A

SHEET 1

22

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

CONNECTIONS ON BARRIER STRIP MX291

*PIN1. SAFTY GROUND.

PIN2 DATA CLOCK OUTPUT REMOTE

PIN3 SHIELD GROUND

PIN4 TO FRONT PANEL BNC DATA OUTPUT

PIN5 DATA OUTPUT — SEE NOTE

PIN6 SHIELD GROUND

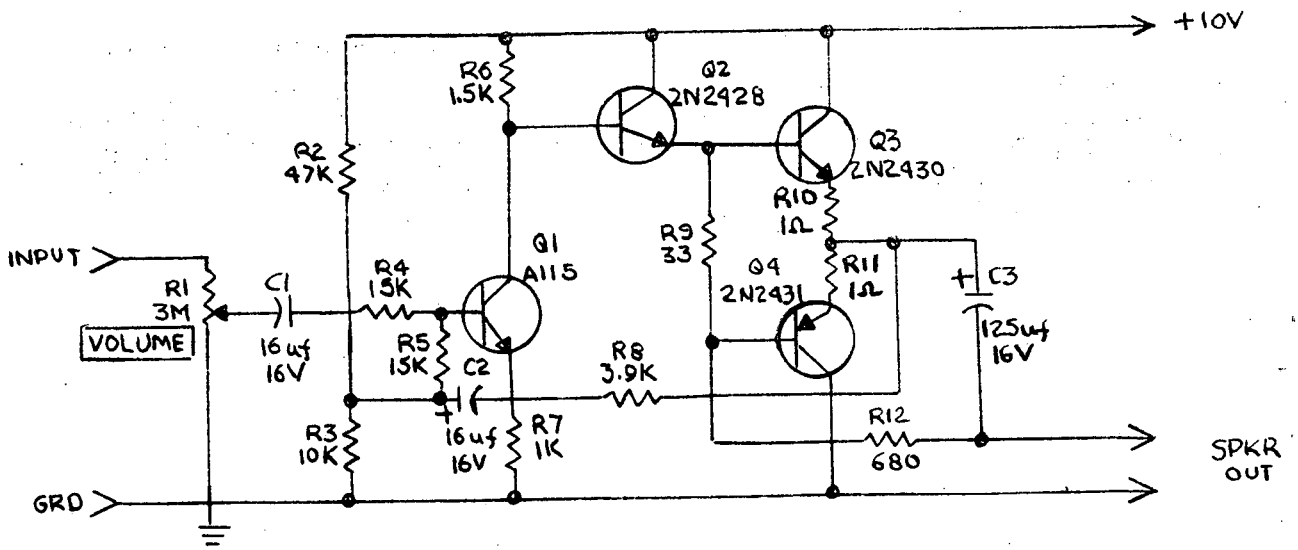
*PIN1 LEFT SIDE WHEN FACING BACK PANEL

NOTE:
TO USE DATA OUTPUT FROM FRONT PANEL BNC JUMPER PIN4 AND 5 TO TAKE DATA OUT FROM BACK PANEL USE PIN 5 AND 6.

23

		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES XXX = ±.010 XX = ±.02 ANGLE = ±0.5°	ORIGN G GILLUM	Magnavox RESEARCH LABORATORIES TORRANCE, CALIFORNIA	
			CHK J. BYROADS		
			APVD M Moran		
			APVD	BARRIER STRIP CONNECTIONS MX 291	
		MATERIAL	APVD		
	MX291		CONTR. DEGN. APPVL.		
NEXT ASSY	USED ON	FINISH	GOVT. CONTR. NO.	SIZE A / CODE IDENT NO 12813 / DRAWING NO SK-42-021	
APPLICATION			GOVT ACTIVITY APPROVAL	SCALE / DWG LEVEL / SHEET 1 OF	

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL
	X1	PROTOTYPE RELEASE @ 9-27-71		



SIGNATURE	DATE
DR G Gillum	9-27-71
CHK	
APP	
APP	
APP	

Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

DIAGRAM SCHEMATIC
SPEAKER AMPLIFIER
MX 291

USED ON / NEXT ASSY	CODE IDENT NO.	SIZE	DWG NO.
TOLERANCE	12813	A	SK42-022
	SCALE N/A		SHEET 1 OF

MRL-66750

APPENDIX A

DEFINITION OF SYMBOLS AND TERMS

Term	Definition
SQPM	Staggered quadriphase modulation can be formed by the equal summing of two biphase modulated signal that have quadrature phased carriers and quadrature clocked binary data streams. Staggered quadriphase modulation is quadriphase modulation with the added restriction that only a $\pm$ 90 degrees phase shift from each phase transition is allowed (180 degrees takes two transitions in SQPM).
PDM	Pulse Duration Modulation
SCPDM	Suppressed Clock Pulse Duration Modulation is PDM with reference zero axis crossings removed.
Gold Code	A Gold code is formed by the mod-two addition of two preferred pair maximal linear sequence generators of equal length.
PREP	PREP occurs when the front panel PREP button is pushed.
P_1, P_2, P_{13}	P_1 throught P_{13} are the signals from the code selector switches on the front panel that are crossinjected into the 13 coder stages. P_1 is injected into the first stage, P_2 is injected into the second stage, etc. This injection occurs when the initial conditions signal is generated.
Code, $\overline{\text{Code}}$	Code, and $\overline{\text{Code}}$ are the two code streams that come from the coder board. Code and $\overline{\text{Code}}$ are quadrature clocked and represent the same stream displaced in phase by 8191/2 bits.
C_i	C_i is the all ones vector of the 23123 coder.

Term	Definition
Search (S)	S is Search. In the receiver MX-291, the system will search or be in sync. Search implies that the internal reference signal does not correlate with the present received signal. Now, the internal sequence generator (rate clock) operates at a reduced rate until correlation is obtained with a received signal. This reduced rate will cause a received signal of the same sequence to slide through or catch up with this internal sequence. The alternate statement would be that the internal reference generator searches backwards for code correlation of an incoming signal, by operating at a reduced clock rate.
SYNC	Sync implies code correlation has been obtained and the Costas loop is locked and the receiver is not searching for sync.
LOCK	After code correlation, the tracking filter and synchronous detector must track the incoming correlated IF signal. To track , the tracking filter must synchronize the IF signal with the tracking filter VCO. When the tracking filter is tracking (has phase locked the internal VCO with the incoming signal), the system is said to be in lock.
T	Transmit: Tx logical 1 = transmit state Tx logical 0 = stand-by
-12T	The minus 12 volts supply will be actuated for the transmit state and disconnected during the STD-BY state.
TXL	Transmit local: TXL is the mike button control signal or the front panel T/STD-By SW. The phone putton is spring loaded and is normally open. When the button is pushed, contact is made with ground. If TXL is grounded, the system is in transmit mode.

Term	Definition
TXR	Transmit Remote: TXR is the remote. By grounding TXR, the system is set into transmit, and an open (no contact) line sets the system into stand-by.
Data Enable	Data Enable signal, s MX-290 signal, that inhibits the transmission of data for the first eight seconds of transmit.
ED1	ED1 is a MX-291 signal and it is the differentially encoded data.
ED2	ED2 is a MX-291 signal and it is either ED1 if in the data mode or the PDM signal if in the PDM mode.
Composit Data	Composite data signal is the mod-two addition of ED2 and the Gold code.
H	H is the first sync decision signal.
J	J is the second sync decision signal.
K	K is the final sync decision schmitt. When K is a logical one, the system is definitely in sync and lock.
I	I is the filtered version of the inphase channel output of the costas loop tracking filter.
$\_/\overline{I}$	$\_/\overline{I}$ is the schmitted version of the I channel output ($\pm$ 10 V).
$\|I\|$	$\|I\|$ is the absolute value of (I) the inphase component of the Costas loop. This signal is formed by the multiplication of schmitted I with I. Multiplication here is implemented by the linear (chopper) mixer approach, where schmitted I is the L.O. gate or chopper signal. Therefore, implementation of multiplication, here implies algebraic addition of arguments and the modular (magnitude) of the analog signal of the complex signals.
$\|Q\|$	$\|Q\|$ is the absolute value of Q or the magnitude of Q is the magnitude of the quadrature channel signal of the Costas loop.

Term	Definition
I + Q	This signal is the sum of |I| and |Q| which are described in this appendix.
24DR	24DR is MX-291 2400 digital data rate command control signal.
12DR	12DR is the MX-291 1200 digital data rate command control signal.
Vc	Command voltage for the 12 MHz voltage controlled crystal oscillator.

APPENDIX B

PSEUDONOISE COMMUNICATION EQUIPMENT FINAL ACCEPTANCE TEST FOR MX-290 SERIAL NUMBER 102 AND MX-291 SERIAL NUMBER 202

Contract No. NAS 5-16955

Prepared for:

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Prepared by:

Magnavox Research Laboratories
2829 Maricopa Street
Torrance, California 90503
(213) 328-0770

MRL Report No. R-4164
20 September 1971

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

SECTION I

SUMMARY OF NASA SPECIFICATIONS NO. 70327-1

1.1 BASE BAND INPUTS (MX-290)

a. Digital (NRZ), 1200 bps or 2400 bps MIL-STD-188B (applies to Data Modem only).

b. Audio from low impedance microphone or 150 ohm source. Proper amplification shall be provided to allow for preemphasis, AGC and speech conditioning prior to modulation.

1.2 PSEUDO NOISE OUTPUT (MX-290)

a. Center frequency shall be 70 MHz.

b. Power output shall be at least 0 dBm into 50 ohm load.

1.3 CODE (MX-290)

a. Code clock shall be 1.228 mb/s.

b. Code length shall be 8191 bits.

c. Codes available shall be 8192.

1.4 CLOCK OUTPUT (MX-290)

a. External clock outputs at 1200 Hz and 2400 Hz to MIL-STD-188B.

1.5 INPUT POWER (MX-290)

The transmitters shall operate from a 50-60 Hz, 117 Vac, single phase source.

1.6 FRONT PANEL CONTROLS (MX-290)

a. Switches to allow selection of any one of 8192 codes

b. Power off and on switch

c. Bit rate selector switch

d. Sync light

e. Reset button

f. Transmit/receive switch

g. Voice/data switch

1.7 BASE BAND OUTPUTS (MX-291)

The receivers (MX-291) shall perform to the following specifications:

a. Digital NRZ, 1200 or 2400 bps, MIL-STD-188B (applies to data mode only).

b. Clock at 1200 or 2400 bps, MIL-STD-188B (applies to data mode only).

c. Audio output shall provide at least 0 dBm into an 3.2 ohm speaker.

1.8 INPUT (MX-291)

a. Center frequency input shall be 70 MHz.

b. Input impedance shall be 50 ohms.

c. Minimum input level shall not be greater than -78 dBm.

1.9 CODE (MX-291)

a. The clock shall be 1.228 mb/s.

b. The code length shall be 8191 bits.

c. Codes available shall be 8192.

1.10 PERFORMANCE (MX-291)

a. The probability of error shall be at least 10^{-5} for data bit rates of 1200 and 2400 b/s for an input N/S ratio of 15 dB (goal of 17 dB) and 13 dB (goal of 16 dB), respectively, in a 1.22 MHz bandwidth. (Applies to data mode only.)

b. The audio output S/N ratio shall be 14 dB (goal of 15 dB) for an input N/S ratio of 11 dB (13 dB goal) in a 1.22 MHz bandwidth.

c. The track threshold shall be at least 15 dB (goal of 18 dB) N/S ratio in a 1.2 MHz bandwidth. (Applies to data mode only.)

d. In the voice mode the track threshold shall be at least 13 dB (goal 16 dB) N/S ratio in a 1.22 MHz bandwidth.

e. The probability of acquisition per pass shall be at least 90% for an input N/S ratio of 13 dB minimum with a goal of 16 dB in a 1.22 MHz bandwidth. (Applies to data mode only.)

f. In the voice mode, the probability of acquisition per pass shall be at least 90% for an input N/S ratio of 10 dB minimum with a goal of 12 dB in a 1.22 MHz bandwidth.

g. Acquisition time shall not be greater than 10 seconds. (Same for both data and voice modes.)

1.11 INPUT POWER (MX-291)

The receivers shall operate from a 50-60 Hz, 117 Vac, single phase source. (Same for both data and voice modes.)

1.12 FRONT PANEL CONTROLS (MX-291)

a. Switches to allow selection of any one of 8192 codes
b. Power off and on switch
c. Bit rate selector switch
d. Voice/Data switch

1.13 MX-290-291 SYSTEM

The audio frequency response for the system shall be 300 Hz to 2.5 kHz +1 dB, -3 dB.

SECTION II
INTRODUCTION

Acceptance tests of the MX-290 Transmitter and the MX-291 Receiver relative to NASA Goddard Space Center Specification N070327-1 were performed at MRL by Mr. Ralph Miller (NASA), Mr. Malcolm M. Lorang (MRL) and Mr. George Gillum (MRL) during the period from 10 May 1971 to 13 May 1971.

2.1 PURPOSE

This document provides a record of various acceptance test results that were performed during the period described above, and will be added to the Final Report.

These results represent what is considered consistent, obtainable results after a period of general testing and observation of system operational characteristics.

Test Equipment Used

Name	Manufacturer	Model
Scope	Tektronix	585
Scope Plug-In	Tektronix	82
Counter	Dana	8130
RF Millivoltmeter	HP	411A
DC Voltmeter	HP	412A
Audio Since Wave Generator	HP	200 CD
True rms Voltmeter	Fluke	910A
RF Generator	HP	809 CE
Spectrum Analyzer	HP	8553L
Wave Analyzer	HP	312A
Attenuators	Kay	30-0 432D

SECTION III
TESTS

3.1 MX-290 DIGITAL INPUT SENSITIVITY

The digital input sensitivity requirement is specified by MIL-STD-188B, paragraph 3.2.4.1.1.6. Sensitivity was obtained by determining the input sinusoid level required to generate a square wave at the point where the data input is reclocked.

3.1.1 TEST EQUIPMENT REQUIRED

Scope	Tek 585
Sine Wave Generator	HP 200CD

3.1.2 TEST PROCEDURE

Connect the HP 200CP to the data input and the Tektronix 585 scope probe to U5, Pin 11 on J103. Start with the signal generator at minimum output and increase the magnitude until a square wave is obtained on the scope. Record the input level at J103 TP1.

3.1.3 TEST RESULTS

A 100-millivolt peak-to-peak signal was measured at the data input test point (J103 TP1).

3.2 MX-290, MX-291 DIGITAL OUTPUT SIGNALS

Specification MIL-STD-188B, paragraphs 3.2.4.1.1.1 and 3.2.4.1.1.3 state the output requirements. The output logic levels and rise and fall times were measured with the Tektronix 585A scope with a Type 82A plug-in.

3.2.1 TEST RESULTS

OUTPUT (DATA/CLOCK)

MX-290 CLOCK OUTPUT

LOGIC ONE LEVEL	+6.2 volts
LOGIC ZERO LEVEL	-6.5 volts
RISE TIME	20 usecs
FALL TIME	22 usecs

MX-290 CLOCK OUTPUT

LOGIC ONE LEVEL	+6.2 volts
LOGIC ZERO LEVEL	-6.2 volts
RISE TIME	34 usecs
FALL TIME	36 usecs

MX-291 DATA OUTPUT

LOGIC ONE LEVEL	+6.2 volts
LOGIC ZERO LEVEL	-6.2 volts
RISE TIME	24 usecs
FALL TIME	20 usecs

3.3 MX-290 70-MHz POWER OUTPUT

Power output requirement is 0 dBm into 50 Ω. Power output was measured by a HP 411A RF Millivoltmeter terminated with 50Ω (Amphenol 46650-51).

3.3.1 TEST RESULTS

Power Output +6 dBm

3.4 MX-290 70 MHz CARRIER FREQUENCY VS. CONTROL SIGNALS

The MX-290 carrier frequency was measured with the MX-290 in narrowband (NB) by a Dana Counter. The DC voltage on the VCO control line was obtained by a HP 412A DC voltmeter. Each dial setting was also recorded.

3.4.1 TEST RESULTS

Carrier Frequency
Vs.
(Dial Setting/Control Voltage)

Dial Setting	Frequency	Voltage
0.00	69.995101	+4.97
1.00	69.995551	+3.88
2.00	69.996780	+2.88
3.00	69.997908	+1.78
4.00	69.999091	+ .75
5.00	70.000384	- .28
6.00	70.001760	-1.32
7.00	70.003001	-2.32
8.00	70.004064	-3.34
9.00	70.004907	-4.36
10.00	70.005540	-5.39

3.5 MX-291 CODER CLOCK FREQUENCY

The MX-291 coder clock frequency was obtained with a Dana Counter for (1) one second and (10) ten second counts:

3.5.1 DATA RESULTS

1 second count	2457300.30 Hz	±2 Hz
10 second count	2457300.24 Hz	
	2457300.29 Hz	
	2457300.26 Hz	
	2457300.23 Hz	
	2457300.21 Hz	
	2457300.21 Hz	

3.6 MX-291 SENSITIVITY

The sensitivity test was conducted by determining the minimum input 70 MHz signal level required for the receiver (MX-291) to sync and maintain lock.

3.6.1 TEST PROCEDURE

The input signal level from a MX-290 was varied by two Kay attenuators to obtain sensitivity levels. After the sensitivity level was obtained, a HP 411 meter was used to obtain the voltage level at the junction of the two attenuators. Sensitivity was defined as the level measured by the meter, down by the attenuation.

3.6.2 TEST RESULTS

The minimum input level is less than -80 dBm.

3.7 MX-291 AUDIO DEMOD TRANSFER FUNCTION

The MX-291 audio demod transfer function was obtained by observing the audio output level vs. frequency for 100% modulation at all frequencies.

3.7.1 TEST EQUIPMENT REQUIRED

Audio Sine Wave Generator	HP 200CD
RMS Voltmeter	Fluke 910
Scope	Tektronix 585
RF Attenuators	Kay 30-0-432D

3.7.2 TEST PROCEDURE

The input level to the MX-291 was set to -60 dBm via Kay attenuators. The 200CD was connected to the audio input jack. The rms voltmeter to J207-TP9 and the scope to J104-TP4. The audio input was increased to the point where the modulation was 100% for each selected audio frequency, and the output voltage was obtained from the rms meter.

3.7.3 TEST RESULTS

Frequency	Voltage at TP9
1 kHz	-8.7 dB
1.5 kHz	-10.4 dB
2.0 kHz	-12.7 dB
2.5 kHz	-16.2 dB
3.0 kHz	-31.8 dB
900 Hz	-8.3 dB
800 Hz	-8.0 dB
700 Hz	-7.1 dB
600 Hz	-6.5 dB
500 Hz	-6.1 dB
400 Hz	-5.7 dB
300 Hz	-5.7 dB
200 Hz	-7.0 dB
150 Hz	-8.0 dB
100 Hz	-11.5 dB

3.8 MX-290, MX-291 AUDIO FREQUENCY RESPONSE

The audio frequency response for the MX-290, MX-291 system was obtained by injecting a given sinusoid at the transmitter and recording the rms audio out across the MX-291 receiver speaker coil. The 70 MHz input was set to -60 dBm for the above measurement also.

3.8.1 TEST EQUIPMENT REQUIRED

Audio Sinusoid Signal Generator	HP 200CP
RMS Voltmeter	Fluke 910

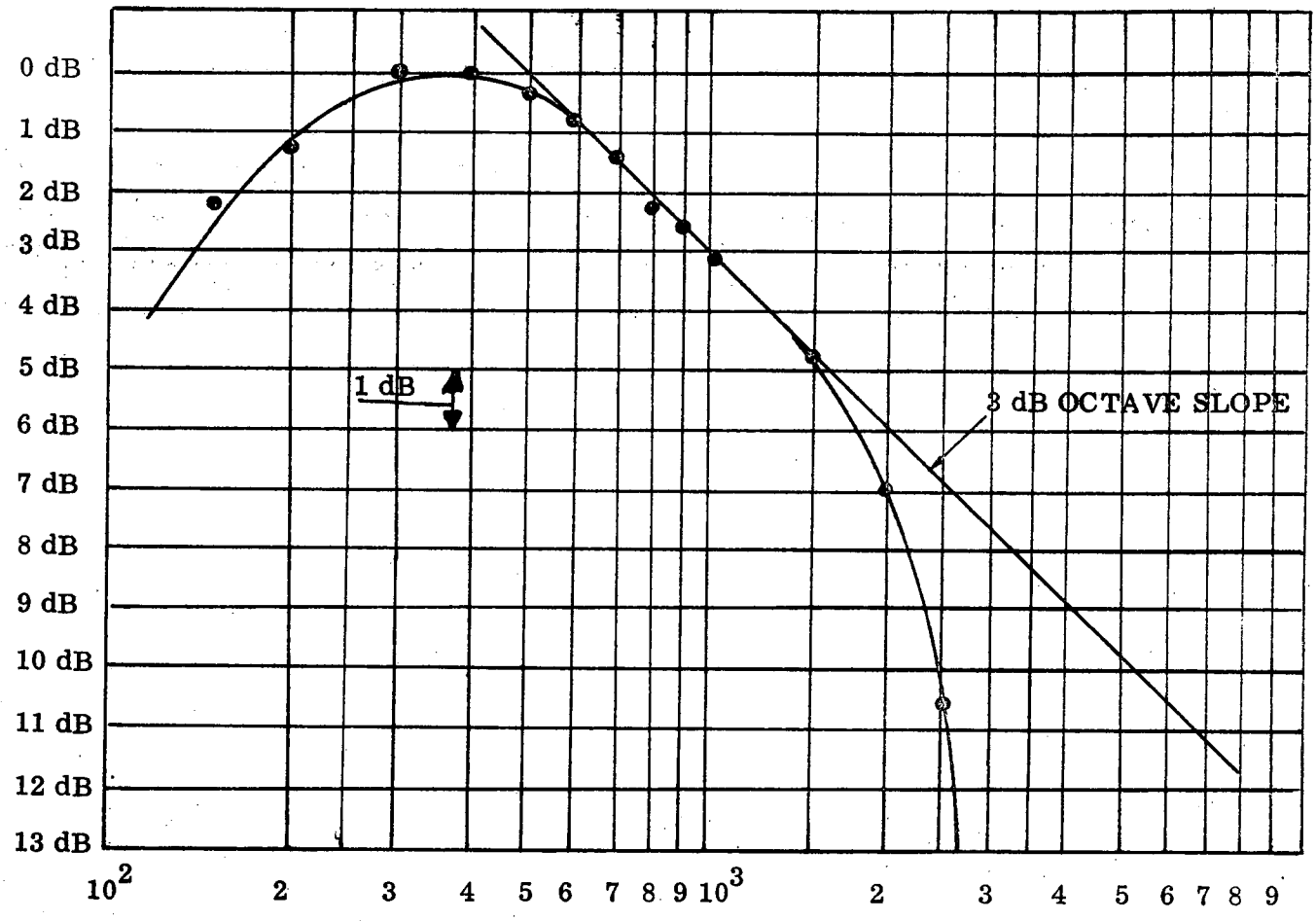
3.8.2 TEST PROCEDURE

The HP 200CD level was selected so that no limiting in the overall audio system could occur. The signal generator input level was held to a constant input magnitude for all frequencies while the audio output level was obtained via the Fluke voltmeter connected across the receiver voice coil.

3.8.3 TEST RESULTS

Frequency	Loss From 1 kHz
100 Hz	-11.0 dB
150 Hz	-7.5 dB
200 Hz	-4.0 dB
250 Hz	-2.2 dB
300 Hz	-1.1 dB
400 Hz	-0.2 dB
500 Hz	+0.2 dB
600 Hz	+0.5 dB

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



● = TEST DATA POINT

SIGNATURE	DATE
DR G. GILLUM	9/9/71
CHK	
APP M. LORANG	5/14/71
APP R. MILLER (NASA)	5/14/71
APP	

Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

AUDIO FREQUENCY RESPONSE OF MX-291 DEMOD
(SERIAL NO. 202)

USED ON NEXT ASSY	CODE IDENT NO.	SIZE	DWG NO.
NA	12813	A	B-9
TOLERANCE NA	SCALE 1/1		SHEET 1 OF

MRL-66750

3.8.3 TEST RESULTS (continued)

Frequency	Loss From 1 kHz
700 Hz	+0.2 dB
800 Hz	+0.4 dB
900 Hz	+0.5 dB
1 kHz	+0.5 dB
1.5 kHz	+0.5 dB
2.0 kHz	+0.2 dB
2.5 kHz	-0.2 dB
3.0 kHz	-13.0 dB
2.75 kHz	-8.0 dB
2.60 kHz	-4.0 dB

3.9 MX-291 TRACKING AND THRESHOLD (HOLD-ON)

The tracking threshold level is expressed by the interference to signal ratio level required to cause the receiver to break lock. The form of interference signal used in this test was another MX-291 transmitter set to a different code.

3.9.1 TEST PROCEDURE

The signal transmitter level was set at -60 dBm and the interference transmitter power level was increased by one dB steps until the receiver breaks lock. The I/S level prior to loss of lock would then be the tracking threshold. Loss of lock is observed by the loss of sync light.

3.9.2 TEST RESULTS

Tracking threshold is greater than 22 dB (I/S) for all modes of operation.

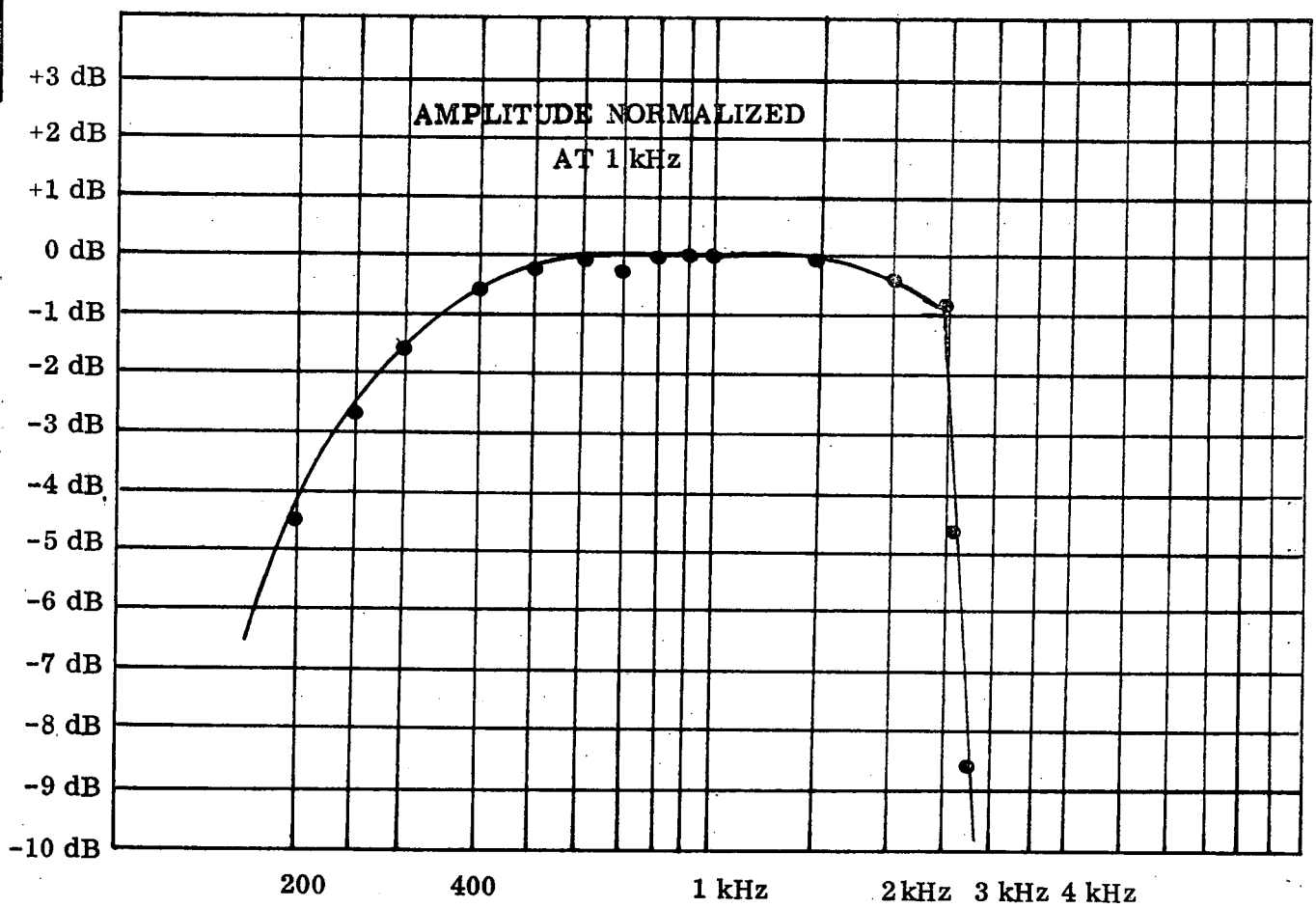
3.10 MX-291 ACQUISITION TIME

Acquisition time is the time interval between initiation of transmit and the indication of sync.

3.10.1 TEST PROCEDURE

A Dana counter was connected to (T), the transmit signal of the MX-291 transmitter; when the sync light came on, the time interval on the counter was recorded. Also, a 585 scope, with a Type 82A plug-in, was connected as follows: (1) sync input from J201-TP6 (Rx all ones vector), (2) signal input from J102-TP1 (Tx all ones vector). This connection shows how the coders slide into correlation and would indicate the number of passes required to sync.

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



SIGNATURE		DATE
DR	G. GILLUM	9-9-71
CHK		
APP	M. LORANG	5-19-71
APP	R. MILLER NASA	5-19-71
APP		

Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

AUDIO FREQUENCY RESPONSE MX-290, MX-291 SYSTEM
(SERIAL NO. 102 AND 202)

USED ON NEXT ASSY	CODE IDENT NO.	SIZE	DWG NO.
NA	12813	A	B-11
TOLERANCE NA	SCALE 1:1		SHEET 1 OF

MRL-66750

3.10.2 TEST RESULTS

The system acquired sync in the first pass for the following I/S ratios and time intervals.

ACQUISITION TIME IN SECONDS

(1 I/S) dB	(1 I/S) dB	Seconds
	15	7,3,7,4,1,7,10,7,1
	16	3,3

3.11 MX-291 AUDIO OUTPUT SIGNAL TO NOISE RATIO $(S/N)_o$ VS. INPUT INTERFERENCE TO SIGNAL RATIO $(I/S)_i$

The transmitted information audio signal is a 1 kHz sinusoid test tone. This test tone is measured at the speaker output coil of the MX-291 receiver with a Fluke 910 true rms voltmeter.

3.11.1 TEST PROCEDURE

The test tone signal is first set to approach a 100% modulation condition. The (I/S) ratio is set by Kay attenuator and a HP 411A RF multivoltmeter terminated with $\overline{50\Omega}$ (Amphenol 46650-51).

This test tone is then applied for a given I/S input, then removed. The difference in dB measured by the Fluke is the recorded output signal plus noise to noise ratio.

3.11.2 TEST RESULTS

Tabulated below are the test results:

(I/S) dB In	(S/N) dB Out	Signal Level Input
0	25	-40 dBm
5	22	-40 dBm
10	18	-40 dBm
11	17	-40, 50 dBm
12	16	-60 dBm
13	15	-60 dBm
14	13	-60 dBm
15	12.5	-60 dBm
16	11	-60 dBm
17	10	-60 dBm

3.11.2 TEST RESULTS (Continued)

(I/S) dB In	(S/N) dB Out	Signal Level Input
18	9.5	-60 dBm
19	8.0	-60 dBm
20	7	-60 dBm

3.12 MX-291 ERROR RATE PERFORMANCE

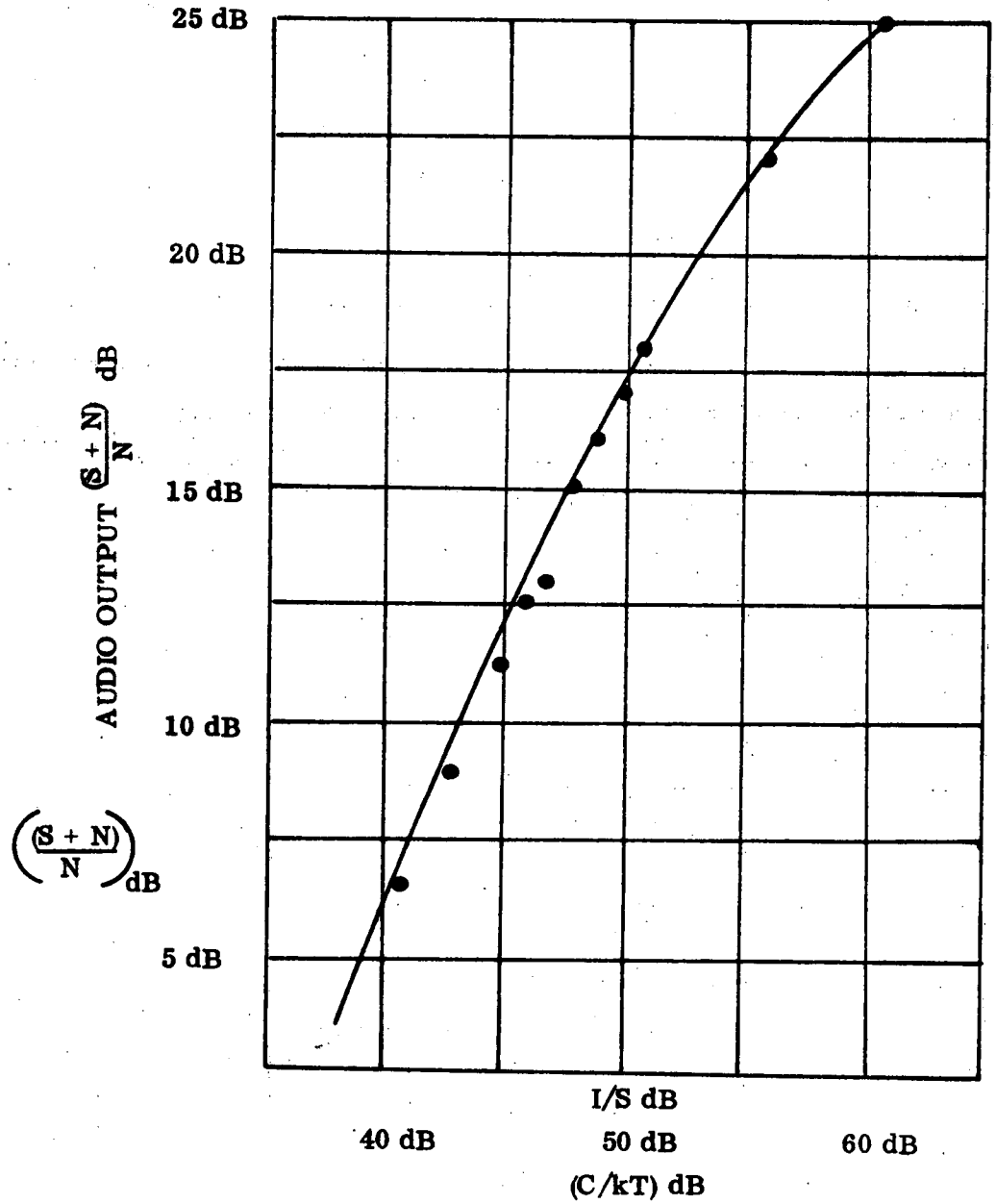
Error rate performance data was obtained by using the MX-270 with the data switch in the long position. This set-up will give a 2047 bit run length data stream generated by a eleven stage maximal linear sequence generator. The signal input power was set a -60 dBm and the interference MX-290 signal was varied to obtain the required I/S ratic. I/S ratios were observed to threshold to obtain a general feeling of the system characteristics. Data was obtained at I/S ratios of 20 and 17 dB which represent a E_{bit}/N_o of approximately 10 dB. The following data represent the number of errors per run generated for 100,000 bits per run. RFI was considered to be the cause for the 10 at 1200, and 14 at 2400.

3.12.1 TEST RESULTS

ERROR RATE MEASUREMENTS

1200 Data Rate 20 dB (I/S) dB Set MX-270 to 10^5 Bits		2400 Data Rate 17 dB (I/S) dB Set MX-270 to 10^5 Bits	
Errors:	0	Errors:	2 4
	1		2 0
	0		0 0
	2		0 4
	0		0 0
	14		10 0
	0		0 0
	7		0 0
	0		0 0
	5		0 0

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



AUDIO OUTPUT (dB)
VS C/kT dB

SIGNATURE	DATE
DR G. GILLUM	9-9-71
CHK	
APP M. LORANG	5/14/71
APP R. MILLER (NASA)	5/14/71
APP	

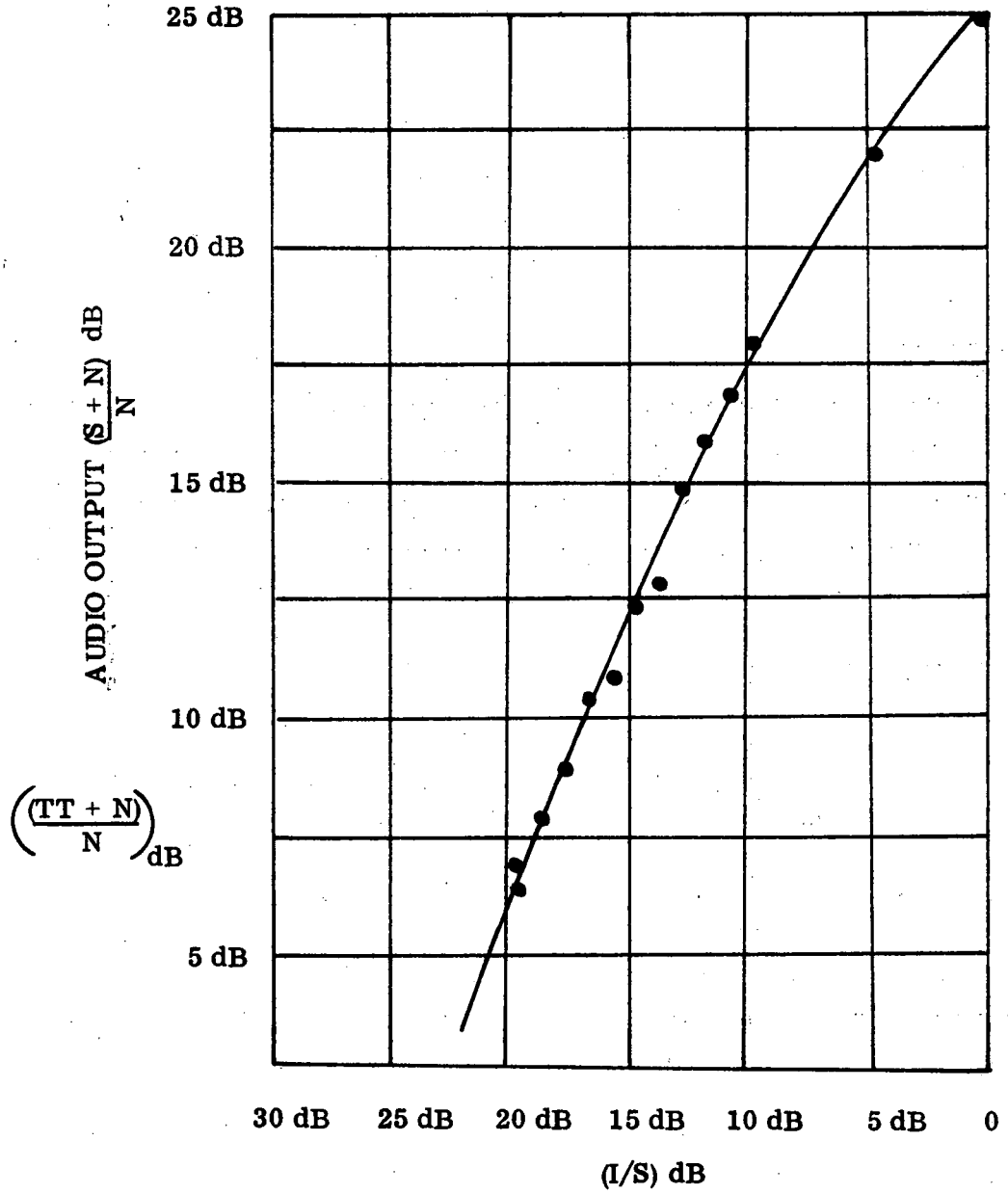
Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

SIGNAL + NOISE TO NOISE
VS.
(C/kT) MX-291 - SERIAL NO. 202

USED ON NEXT ASSY	CODE IDENT NO.	SIZE	DWG NO.
NA	12813	A	B-14
TOLERANCE: NA	SCALE 1:1		SHEET 1 OF

MRL-66750

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



AUDIO OUTPUT (dB) - VS. I/S dB

SIGNATURE	DATE
DR G. GILLUM	9-9-71
CHK	
APP M. LORANG	5-14-71
APP R. MILLER (NASA)	5-14-71
APP	

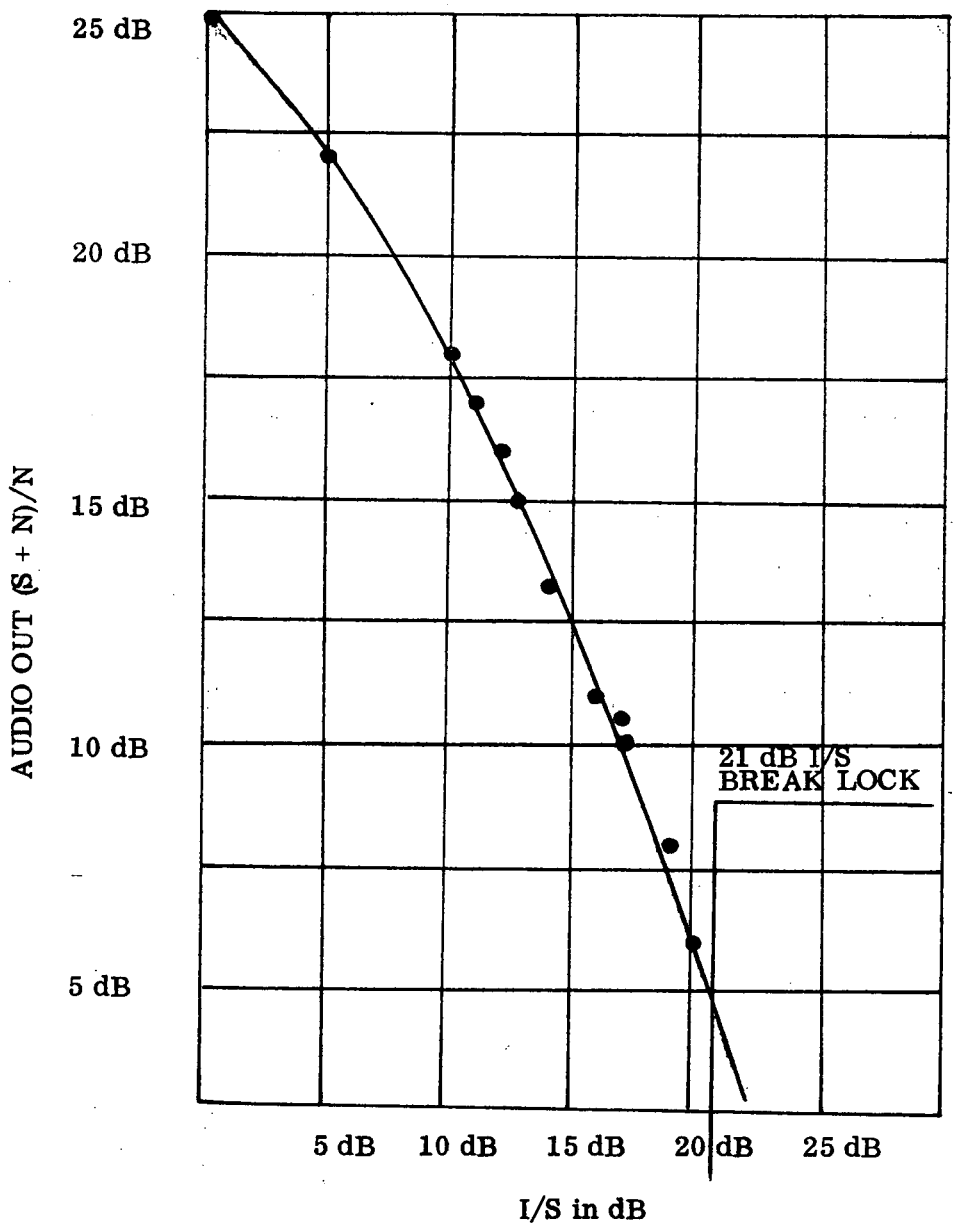
Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

TEST TONE PLUS NOISE TO NOISE
VS.
INTERFERENCE TO SIGNAL - MX-291 SERIAL NO. 202

USED ON NEXT ASSY	CODE IDENT NO.	SIZE	DWG NO.
NA	12813	A	B-15
TOLERANCE NA	SCALE 1:1		SHEET 1 OF

MRL-66750

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



$\frac{(S+N)}{N}$ VS. (I/S)

SIGNATURE	DATE
DR G. GILLUM	9-9-71
CHK	
APP M. LORANG	5/14/71
APP R. MILLER (NASA)	5/14/71
APP	

Magnavox RESEARCH LABORATORIES
TORRANCE, CALIFORNIA

SIGNAL + NOISE TO NOISE
VS.
INTERFERENCE TO SIGNAL

MX-291 SERIAL NO. 202

USED ON NEXT ASSY: NA	CODE IDENT NO. 12813	SIZE A	DWG NO. B-16
TOLERANCE: NA	SCALE 1:1		SHEET 1 OF

MRL-66750